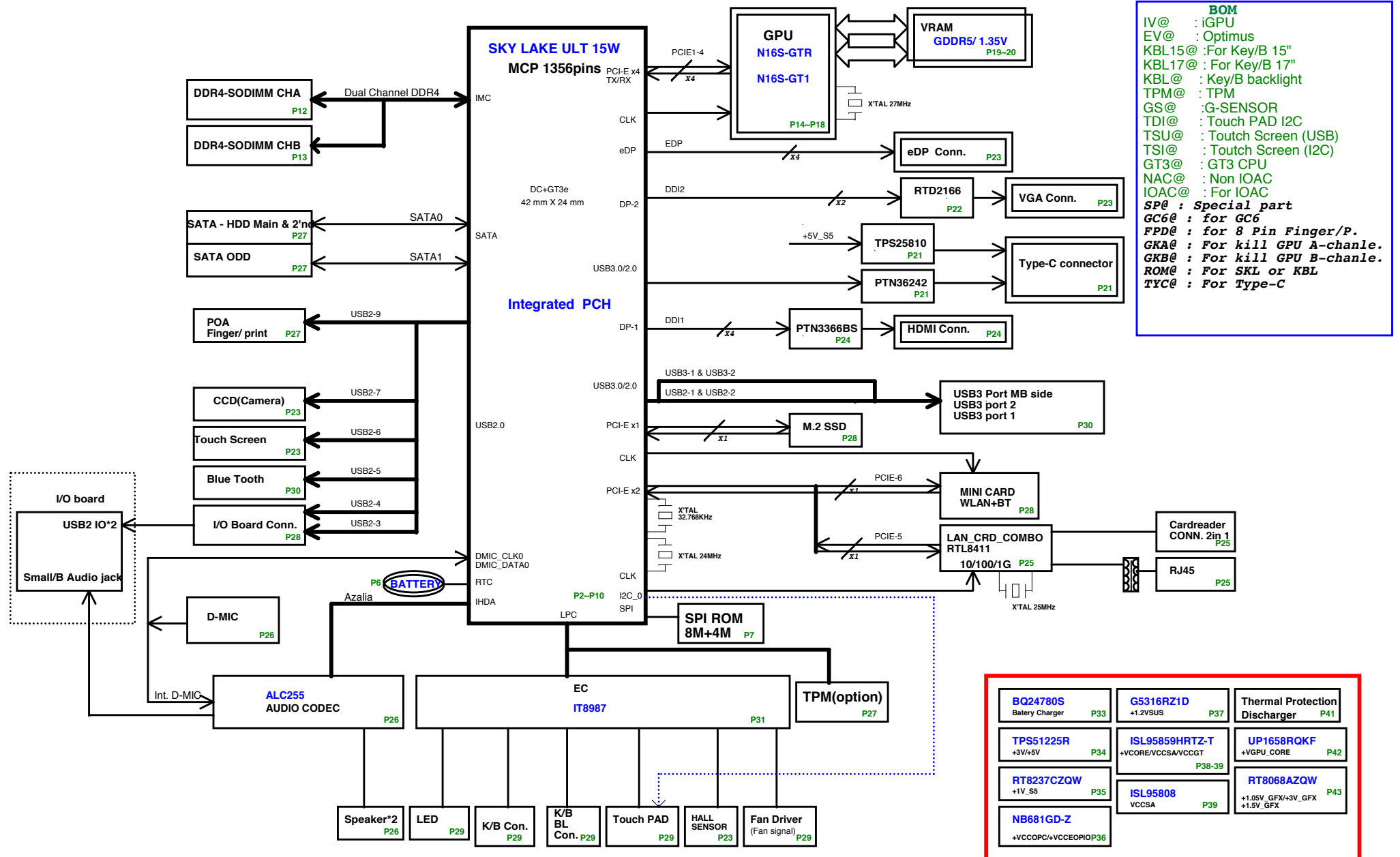


ZAA Serials SKL ULT SYSTEM BLOCK DIAGRAM



```

BOM
IV@      : iGPU
EV@      : Optimus
KBL15@   : For Key/B 15"
KBL17@   : For Key/B 17"
KBL@     : Key/B backlight
TPM@     : TPM
GS@      : G-SENSOR
TDI@     : Touch PAD I2C
TSU@     : Touch Screen (USB)
TSI@     : Touch Screen (I2C)
GT3@     : GT3 CPU
NAC@     : Non IOAC
IOAC@    : For IOAC
SP@      : Special part
GC6@     : for GC6
FPD@     : for 8 Pin Finger/P.
GKA@     : For kill GPU A-chanle.
GKB@     : For kill GPU B-chanle.
ROM@     : For SKL or KBL
TYC@     : For Type-C

```

BQ24780S Batery Charger P33	G5316RZ1D +1.2VSUS P37	Thermal Protection Discharger P41
TPS51225R +3V/+5V P34	ISL95859HRTZ-T +V CORE/VCCSA/VCCGT P38-39	UP1658RQKF +VGPU_CORE P42
RT8237CZQW +1V_SS P35	ISL95808 VCCSA P39	RT8068AZQW +1.05V_GFX/+3V_GFX +1.5V_GFX P43
NB681GD-Z +VCCOPC/+VCCOEPIO P36		

CH6221M9A00	CAP CHIP 22U 6.3V(+20%,X5R,0805)H1.25
CH6221M9A01	CAP CHIP 22U 6.3V(+20%,X5R,0805)H1.25
CH6221M9A02	CAP CHIP 22U 6.3V(+20%,X5R,0805)H1.25




```
remove TPM from SKL , KBL keeps it.---- for B2
add POA FUNCTION , add 0hm*4 between EC to POA conn & server VST * 7 pcs
POA ( change FP power from 3v to 5v )
```

```
i3-6100U  AJSR2EUUT07
i5-6200U  AJSR2EYUT07
i7-6500U  AJSR2EZRT07
i5-6267U  AJSR2JK8T02--no use
```

<u>PU_THRMTRIP#</u>	H_PECI (50ohm)
<u>ATERR#</u>	Route on microstrip only
	Spacing >18 mils
	Trace Length: 0.4~6.125 inches

BPM#[0:7]
Trace Length 1~6 inches
Length match < 300 mils

<4> DGPU_PW_CTRL#

R796		*short 4	XDP_TDI_CPU
R795		*short 4	XDP_TDO_CPU
R797		*short 4	XDP_TMS_CPU

If use Intel DCI USB 3.0 fixture need to short

1. XDP_TDO <=> XDP_TDO_CPU
2. XDP_TDI <=> XDP_TDI_CPU
3. XDP_TMS <=> XDP_TMS_CPU

XDP_TDO	R559	51.4
XDP_TMS	R514	51.4
XDP_TDI	R515	51.4
XDP_TCK0	R513	*1K.4

2/16
XDP_TCK1,XDP_TMS
don't need pull up or pull down

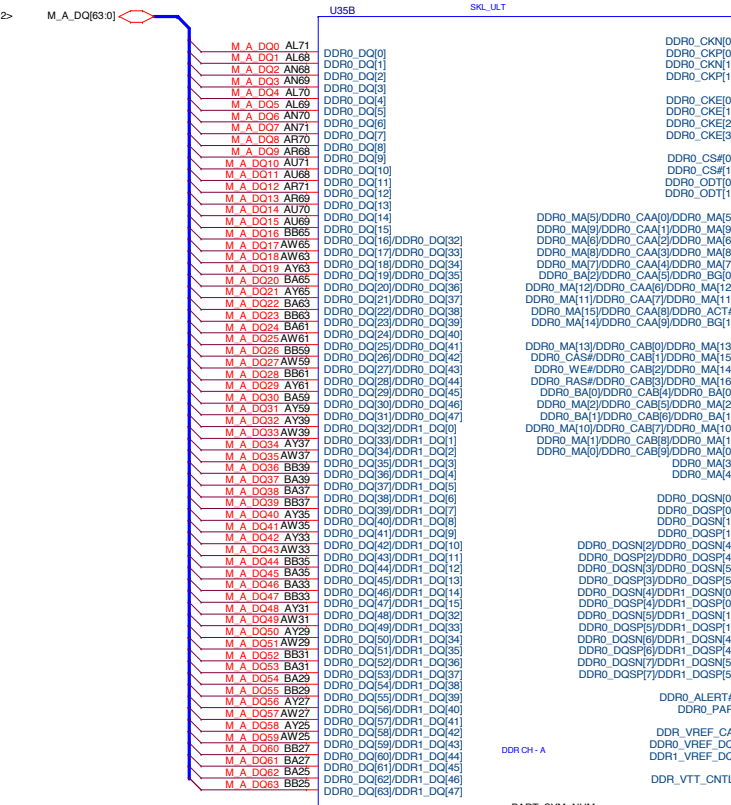
5/29 XDP TCK0 R558 Stuff

[illegible]

+VCCIO <5,8,32,34,37,40>
+1V_VCCST <5,8,9,37>

Change Data and DQS to interleave.

SKL ULT (DDR3L)



SKL ULT (DDR3L)



For Sx, stuff Q? in DDR_VTT_CNTL

DRAM COMP

DRAMRST

CPU

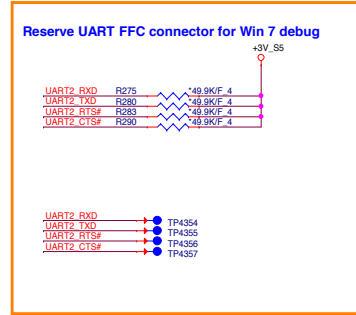
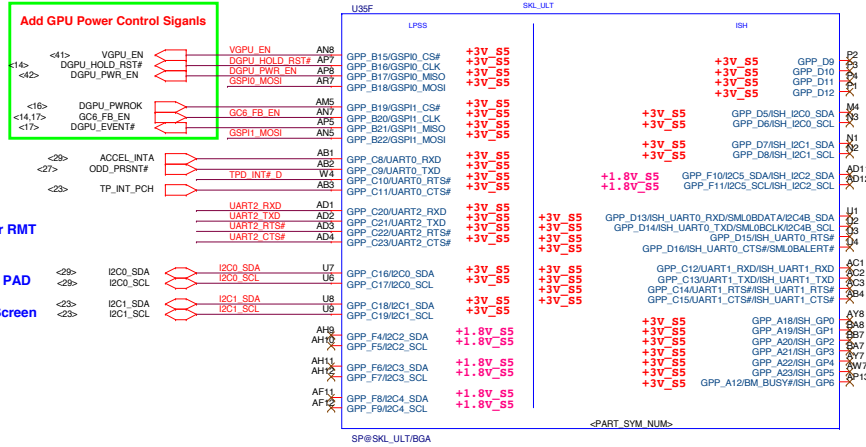
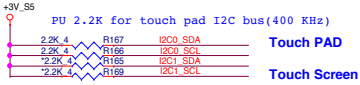
DRAM

www.vinafix.vn

SKL ULT (SIDE BAND) GPIO

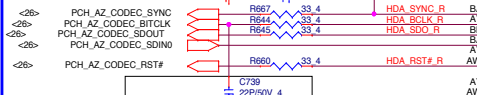
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 inches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

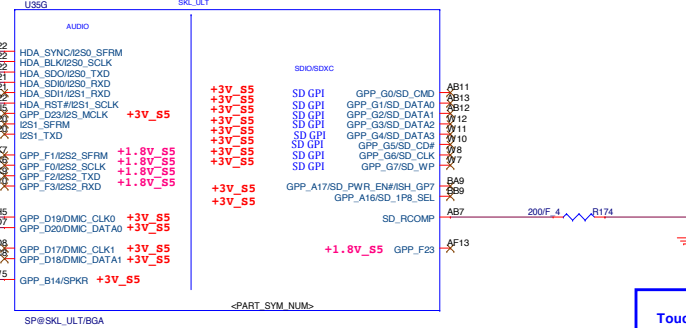


Touch PAD

Touch Screen









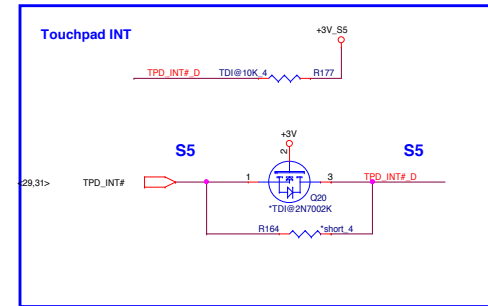
ESD request 2015/12/21

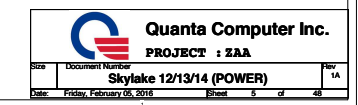


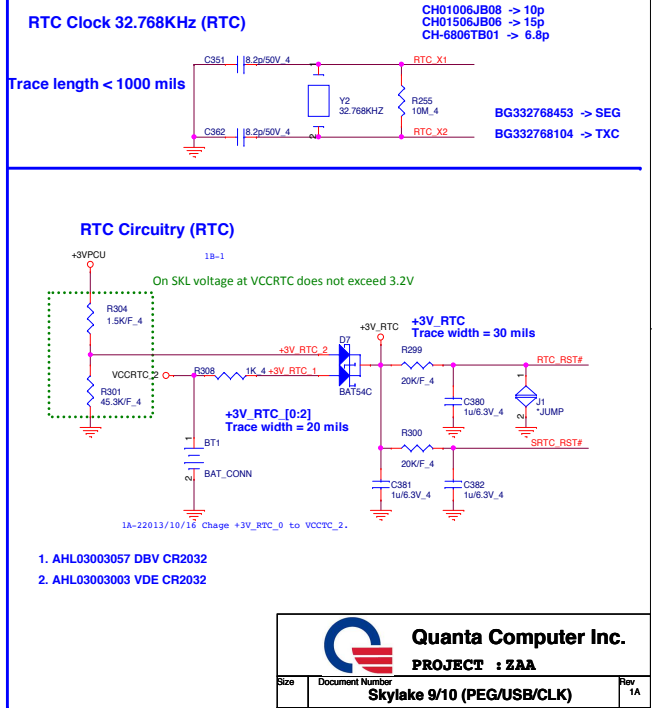
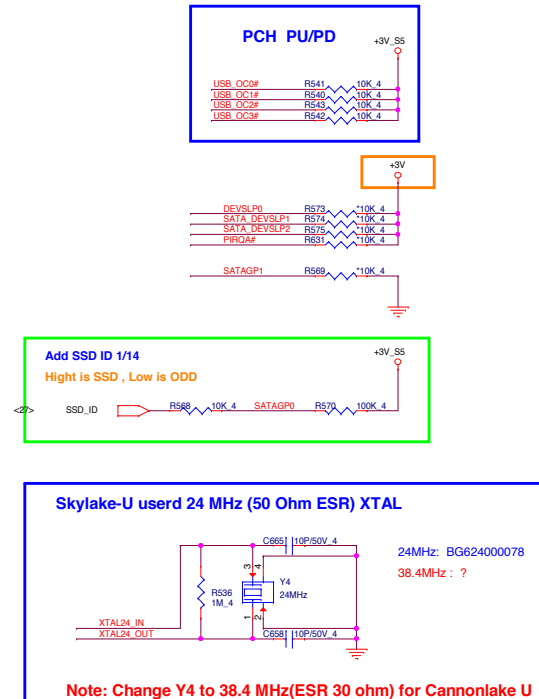
	DGPU_PW_CTRL#	VGA H/W Signal	Setup Menu	
UMA Only	1	UMA	Hidden	UMA boot
SG/Optimise	0	GPU	Hidden	GPU boot

Skylake-U Strapping Table

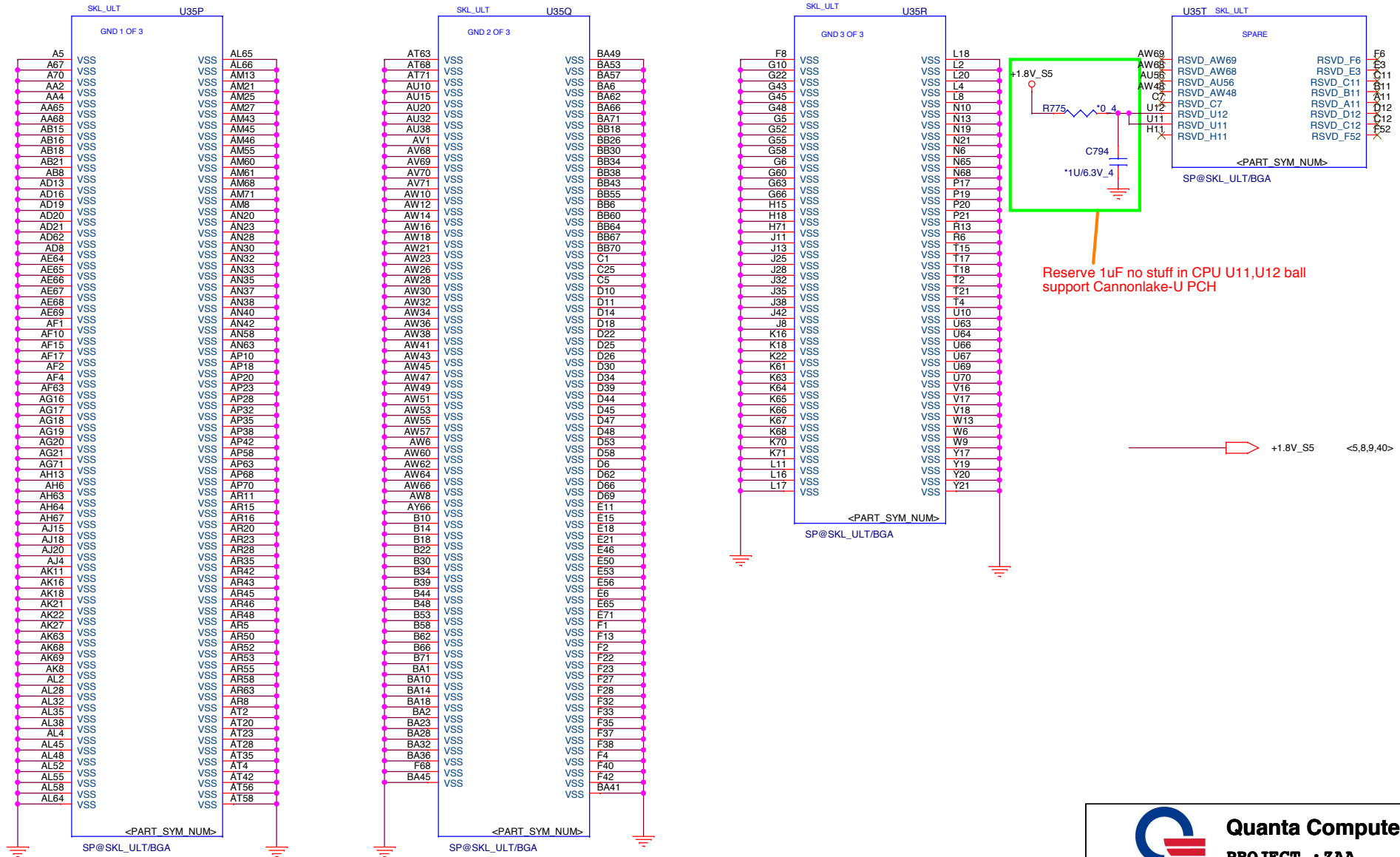
Pin Name	Strap description	Sampled	Configuration	note
GPP_B14 (SPKR)	Top-Block Swap override	PCH_PWROK	0 = *Disable Top Swap (iPD 20K) 1 = Enable Top Swap Mode	+3V  SPKR
GPP_B18 (GSPi0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) 1 = Enable No Reboot Mode	+3V  GSPi0_MOSI
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = *Disable Intel ME Crypt to TLS(iPD 20K) 1 = Enable Intel ME Crypt to TLS	+3V_SS  SMBALERT# <7>
GPP_B22 (GSPi1_MOSI)	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = *SPI (iPD 20K) 1 = LPC	+3V  GSPi1_MOSI
GPP_C5 (SML0ALERT#)	eSPI or LPC	RSMRST#	0 = *LPC is selected for EC (iPD 20K) 1 = eSPI selected for EC	+3V_SS  SML0ALERT# <7>
SPI0_MOSI	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_MISO	Reserved	RSMRST#	(iPU 15 ~ 40K)	
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(iPD 20K)	
SPI0_IO2	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_IO3	Reserved	RSMRST#	(iPU 15 ~ 40K)	
HDA_SDO / I2S_TXD0	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = *Enable security in the Flash Descriptor (iPD 20K) 1 = Disable Flash Descriptor Security (Override)	change location to near CPU to prevent impact HDA_SDO signal  ME_WR# <31>
GPP_E19 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = *Port B is not detected (iPD 20K) 1 =Port B is detected	
GPP_E21 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = *Port C is not detected (iPD 20K) 1 =Port C is detected	







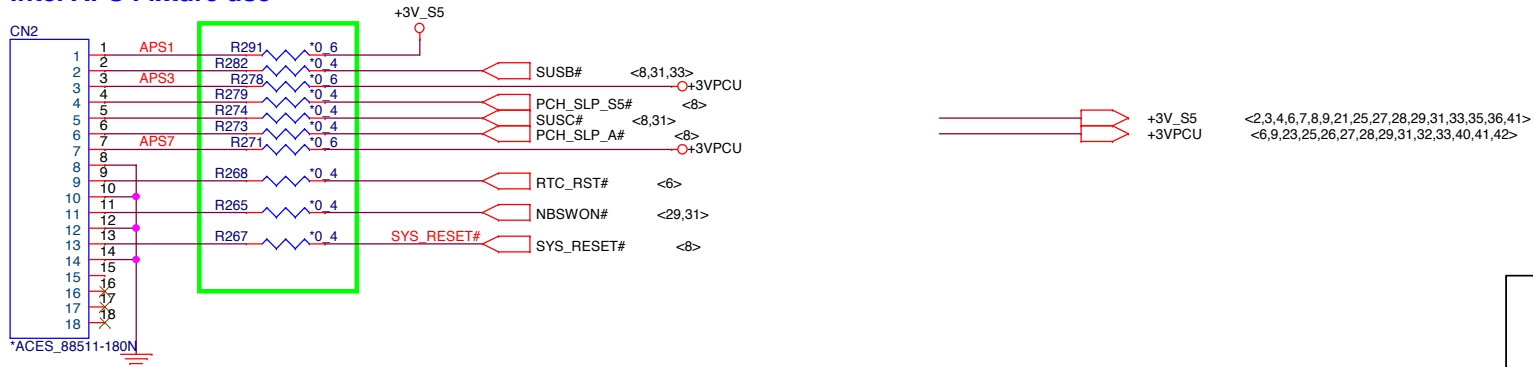
Skylake ULT (GND)

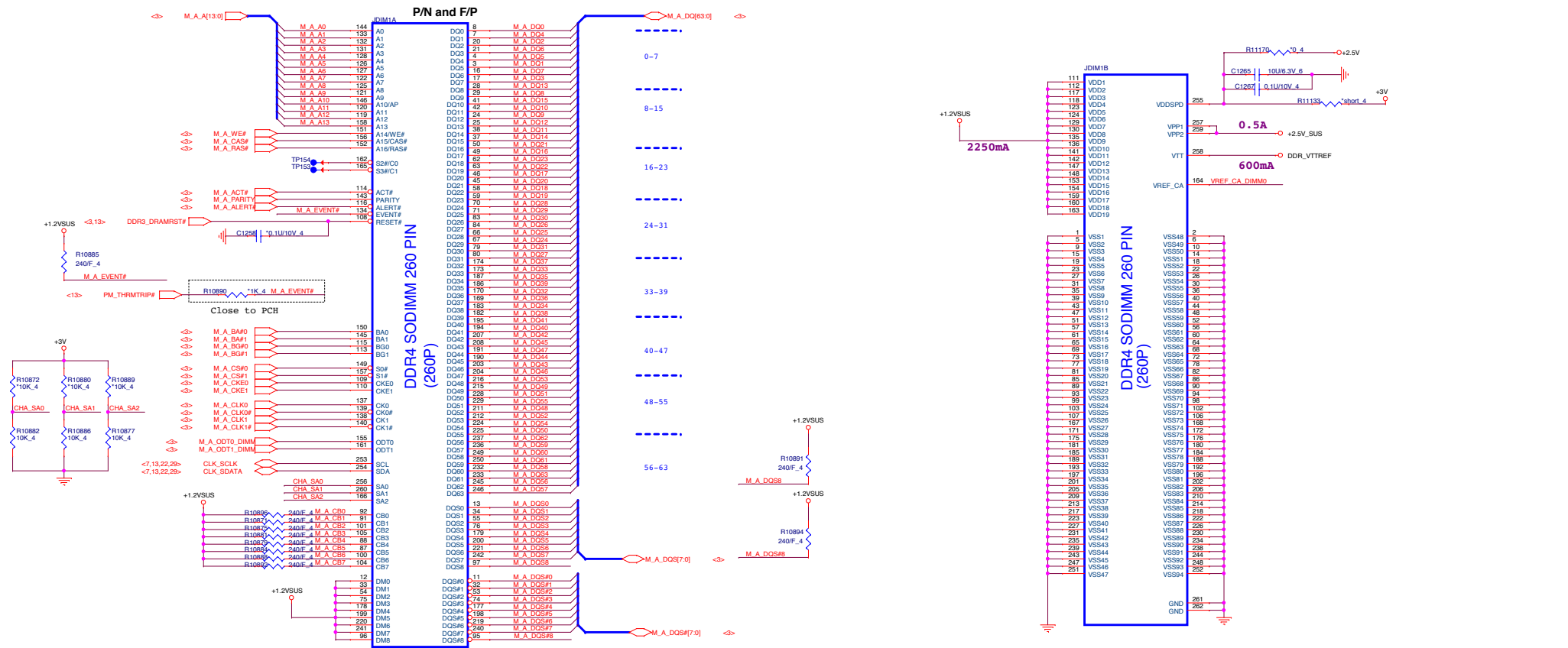


Quanta Computer Inc.
PROJECT : ZAA

Size	Document Number	Rev
	Skylake 10/17/18 (GND)	1A
Date:	Friday, February 05, 2016	Sheet 10 of 48

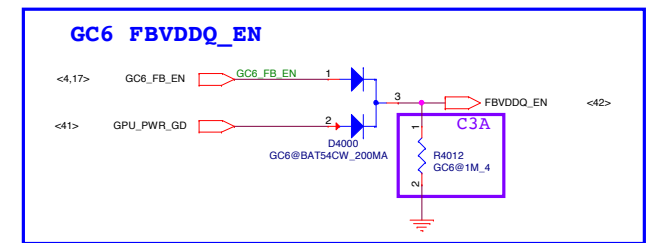
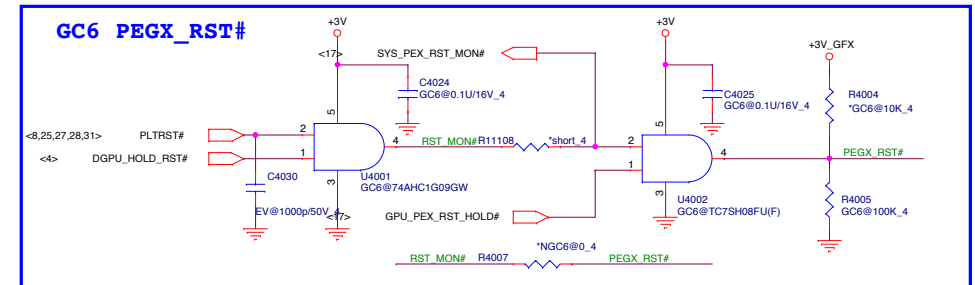
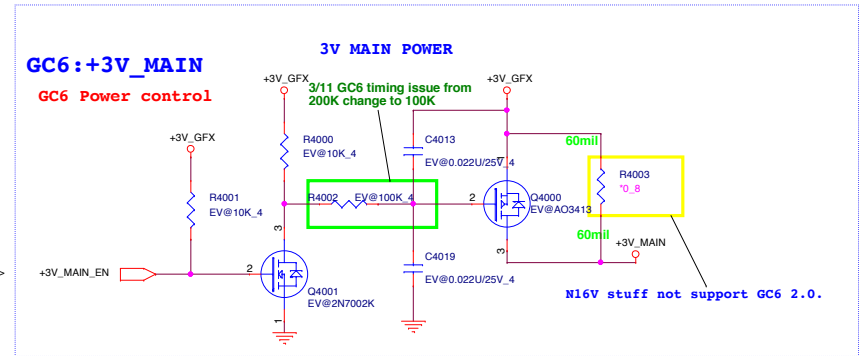
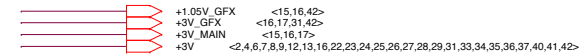
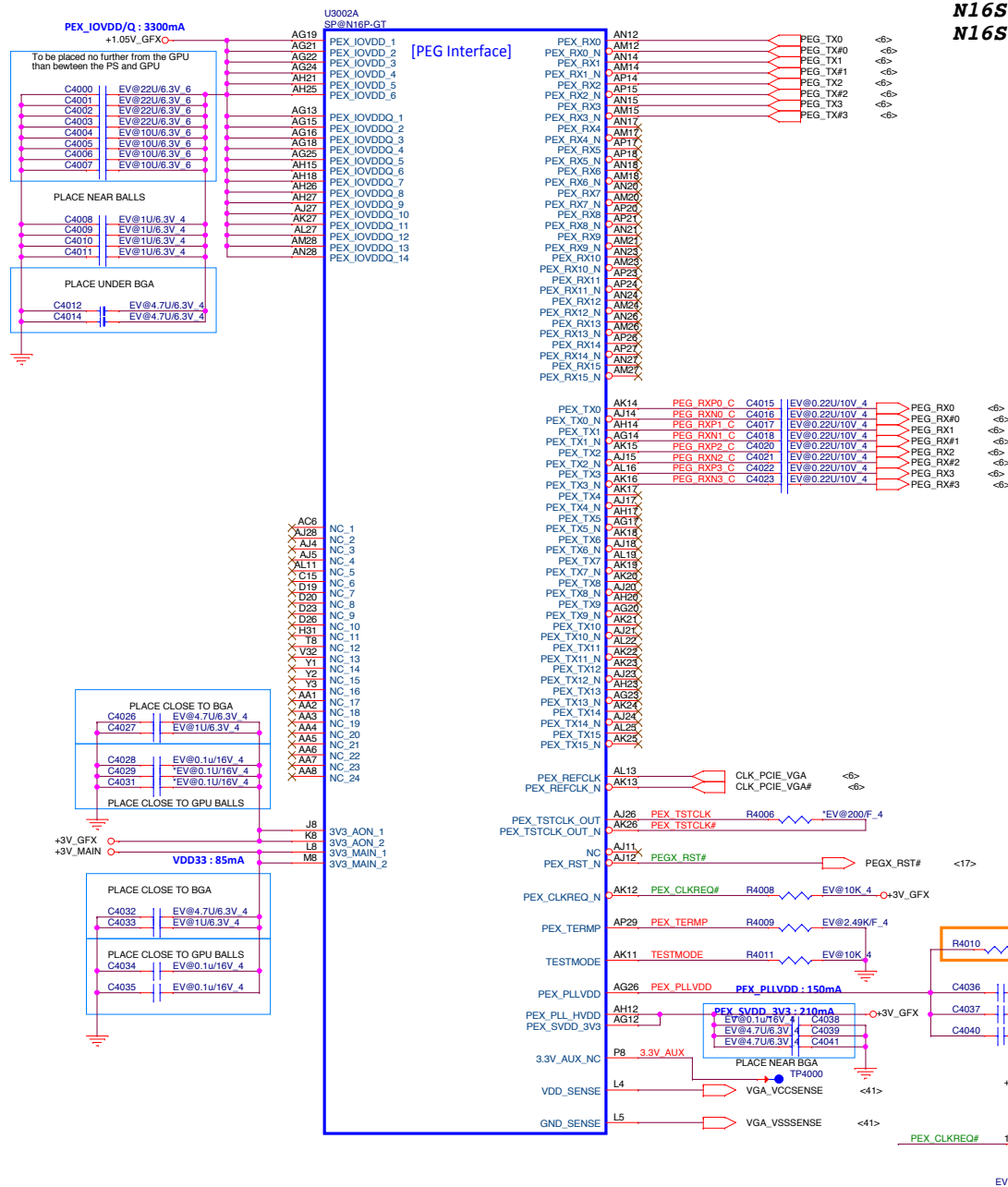
Intel APS Fixture use

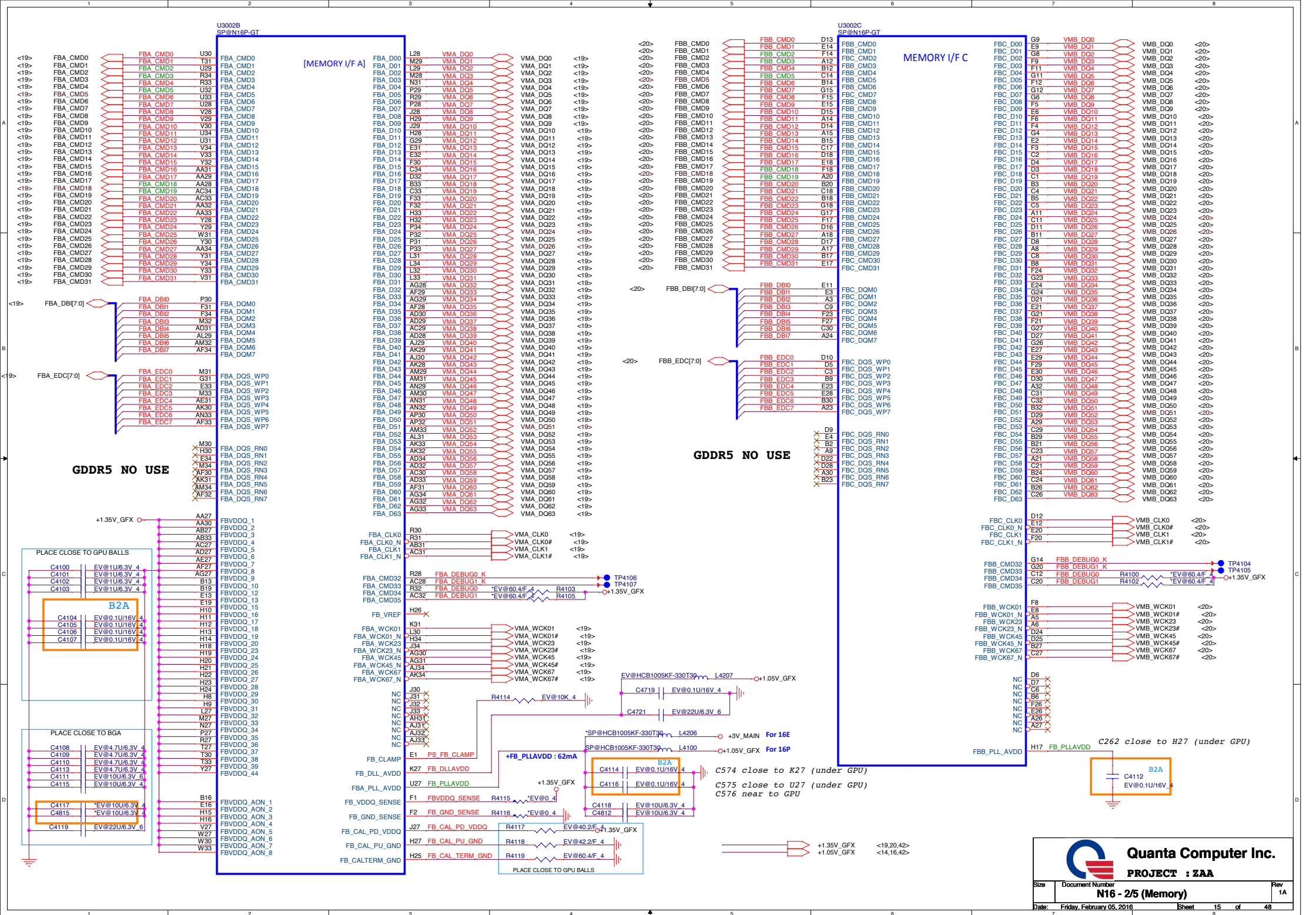




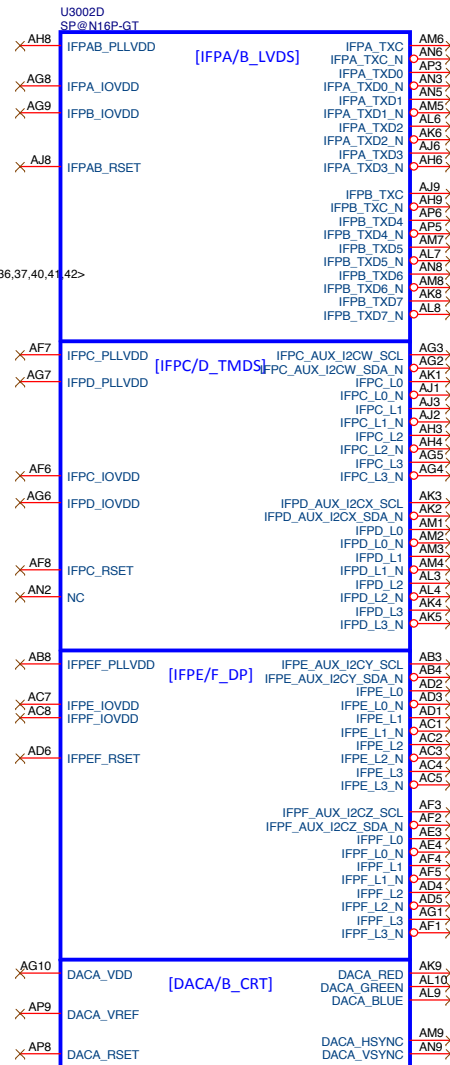
Size	Document Number DDR4 DIMM-RVS(5.2H) CHB	Rev 1A
Date: Friday, February 05, 2016	Sheet 13 of 48	

N16S-GT1-KA-A2 GM107-710-KA-A2 AJON16S0T22 B/S PN
N16S-GT1-KB-A2 GM107-710-KB-A2 AJSR2JK8T02
N16S-GTR-B-A2 GM108-770-A2 AJON16S0T24

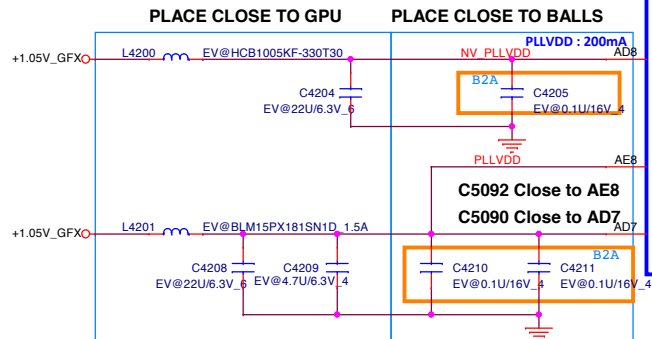
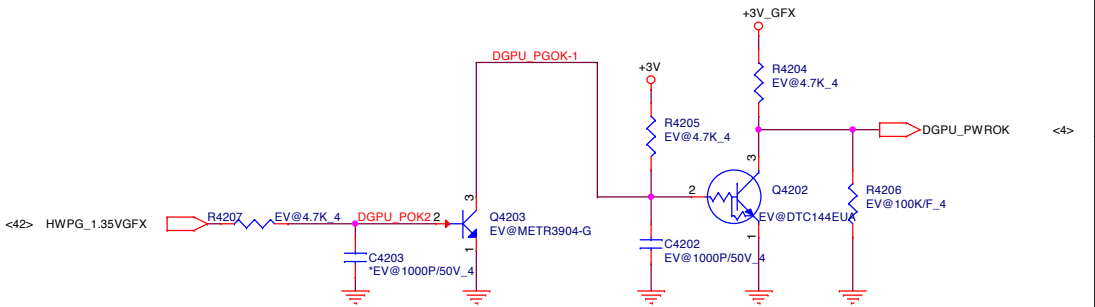
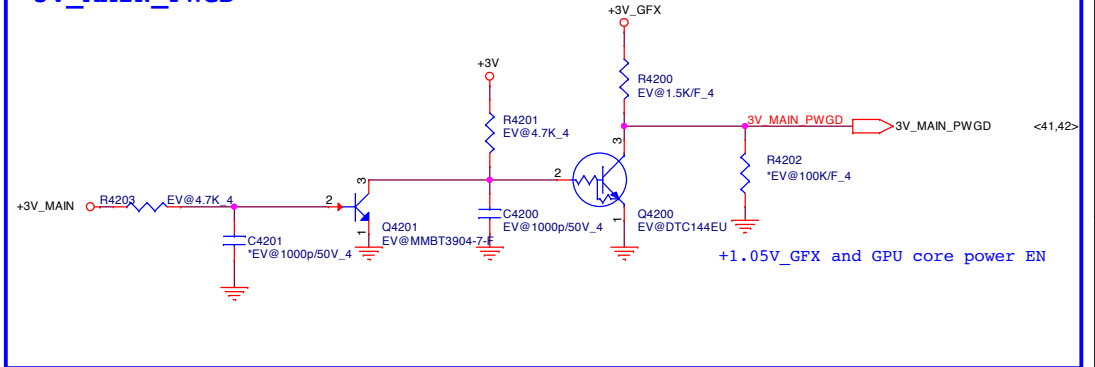




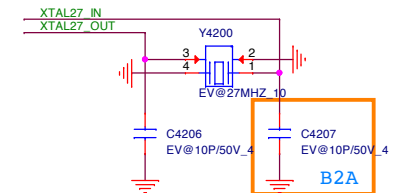
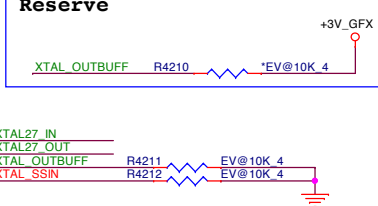
+3V_MAIN <14,15,17>
 +1.05V_GFX <14,15,42>
 +3V_GFX <14,17,31,42>
 +3V <2,4,6,7,8,9,12,13,14,22,23,24,25,26,27,28,29,31,33,34,35,36,37,40,41,42>



3V_MAIN_PWGD



Reserve



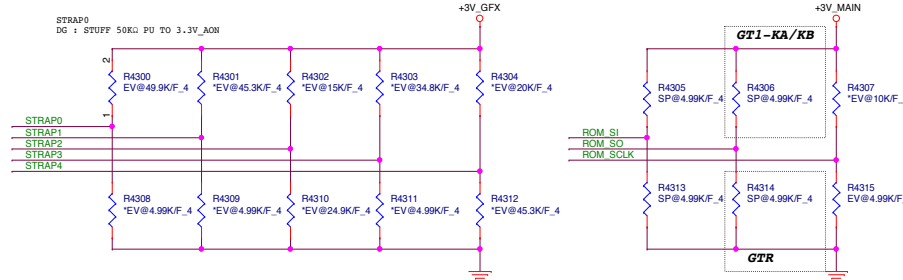
Quanta Computer Inc.
PROJECT : ZAA

Default setting : N16S-GTR, Samsung 4GB

Package	DevID
(default) N16S-GTR	GB4b-128
N16S-GT1-KA	GB4b-128
N16S-GT1-KB	GB4b-128

Resistor P/N
 4.99K ----> CS24992FB26
 10K ----> CS31002FB26
 15K ----> CS31502FB24
 20K ----> CS32002FB29
 24.9K ----> CS32492FB16
 30.1K ----> CS33012FB18
 34.8K ----> CS3482FB22
 45.3K ----> CS34532FB18
 49.9K ----> CS34992FB10

x16 (8L)					
#2					
SKU15 (B6)	SKU16 (B6)	SKU17 (B5)	SKU19 (B5)	SKU18	SKU20
GT3	(B6)				
For VRAM Timing Tuning					
i5-6200U	i7-6500U	i5-6200U	i5-6200U	i5-6200U	i5-6200U
N16S-GTR	N16S-GTR	940M KA	940M KB	940M KA	940M KB
4G	4G	4G	4G	4G	4G
512x16x4	512x16x4	512x16x4	512x16x4	512x16x4	512x16x4
K4G80325FB-HC03 (Samsung)	MT51J256M32HF-60A (Micron)	K4G80325FB-HC03 (Samsung)	K4G80325FB-HC03 (Samsung)	MT51J256M32HF-60A (Micron)	MT51J256M32HF-60A (Micron)



N16S-GTR VRAM Configuration Table: N16S-GTR-B-A2 GM108-770-A2 AJON16S0T24

	ROM_SI	DESCRIPTION	Vendor	Vendor P/N	STN P/N	ROM_SI
4GbX2 (1GB)	0011 (0x3) 0110 (0x6)	GDDR5 128MBx32,2500MHz GDDR5 128MBx32,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5GC4H24AJR-T2C --A die	AKG5PGDT505 AKG5PWUTW21	20K Pull down 34.8K Pull down
4GbX4 (2GB)	0011 (0x3) 0110 (0x6)	GDDR5 256MBx16,2500MHz GDDR5 256MBx16,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5GC4H24AJR-T2C --A die	AKG5PGDT505 AKG5PWUTW21	20K Pull down 34.8K Pull down
8GbX2 (2GB)	0000 (0x0) 0001 (0x1)	GDDR5 256MBx32,2500MHz GDDR5 256MBx32,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60A--A die	AKG5QGDT502 AKG5LGUTL04	4.99K Pull down 10K Pull down
8GbX4 (4GB)	0000 (0x0) 0001 (0x1)	GDDR5 512MBx16,2500MHz GDDR5 512MBx16,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60A--A die	AKG5QGDT502 AKG5LGUTL04	4.99K Pull down 10K Pull down

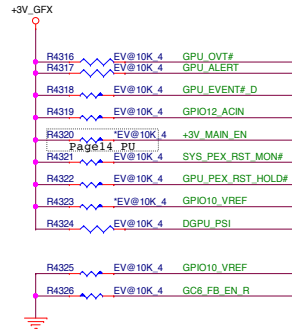
N16S-GT1-KA-KB-A2 VRAM Configuration Table: N16S-GT1-KA-A2 GM107-710-KA-A2 AJON16S0T22
 N16S-GT1-KB-A2 GM107-710-KB-A2 AJON16S0T23

	ROM_SI	DESCRIPTION	Vendor	Vendor P/N	STN P/N	ROM_SI
4GbX2 (1GB)	0011 (0x3) 0110 (0x6)	GDDR5 128MBx32,2500MHz GDDR5 128MBx32,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5GC4H24AJR-T2C --A die	AKG5PGDT505 AKG5PWUTW21	20K Pull down 34.8K Pull down
4GbX4 (2GB)	0011 (0x3) 0110 (0x6)	GDDR5 256MBx16,2500MHz GDDR5 256MBx16,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5GC4H24AJR-T2C --A die	AKG5PGDT505 AKG5PWUTW21	20K Pull down 34.8K Pull down
8GbX2 (2GB)	0000 (0x0) 0001 (0x1)	GDDR5 256MBx32,2500MHz GDDR5 256MBx32,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60A--A die	AKG5QGDT502 AKG5LGUTL04	4.99K Pull up 10K Pull up
8GbX4 (4GB)	0000 (0x0) 0001 (0x1)	GDDR5 512MBx16,2500MHz GDDR5 512MBx16,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60A--A die	AKG5QGDT502 AKG5LGUTL04	4.99K Pull up 10K Pull up

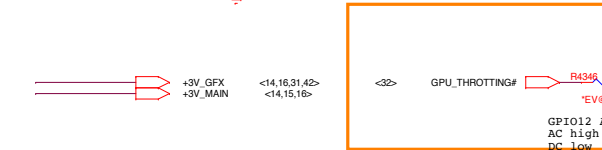
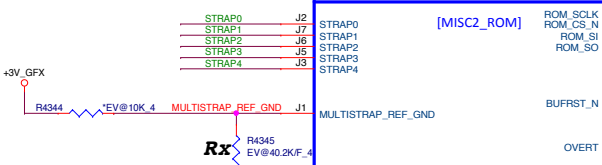
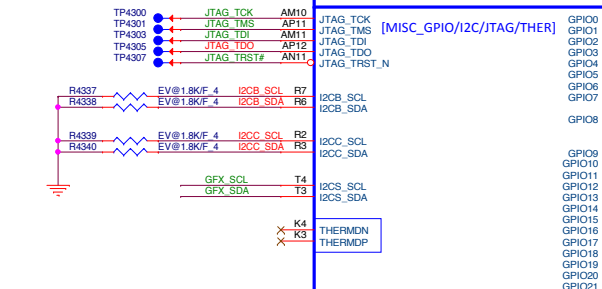
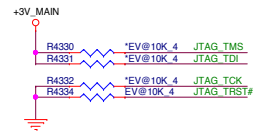
	PU +3V_MAIN	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Mult-level mode strapping:

- Rx=40.2k PD
- ROM_SCLK = 4.99K PD for GTR ; 4.99K UP for GT1-KA/KB
- ROM_SI= VRAM Configuration Table
- STRAP0 = 49.9K PU
- Strap4~1 = Reserve Pull up and Pull down



Reserve PU/PD for Debug



(GB4b-128)					
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	Refer table
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE	0000 ---GTR 1000 ---GT1/KA/KB
STRAP0	Keep footprint to PU to 3V3_AON and PD to GND				[Stuff 49.9K PU]
STRAP1	Keep footprint to PU to 3V3_AON and PD to GND				[Do Not Stuff]
STRAP2					
STRAP3					
STRAP4					



VDD/XVDD : 43A

+VGPU_CORE

U3002F
SP@N16P-GT

[GPU VDD]

XVDD_001
XVDD_002
XVDD_003
XVDD_004
XVDD_005
XVDD_006
XVDD_007
XVDD_008
XVDD_009
XVDD_010
XVDD_011
XVDD_012
XVDD_013
XVDD_014
XVDD_015
XVDD_016
XVDD_017
XVDD_018
XVDD_019
XVDD_020
XVDD_021
XVDD_022
XVDD_023
XVDD_024
XVDD_025
XVDD_026
XVDD_027
XVDD_028
XVDD_029
XVDD_030

+VGPU_CORE

U3002G
SP@N16P-GT

[GPU GND]

A2
AA17
AA18
AA20
AA22
AB12
AB14
AB16
AB19
AB21
AB23
AB28
AB30
AB32
AB35
AB7
AC13
AC15
AC17
AC18
AA13
AC20
AC22
AE2
AE28
AE30
AE32
AE33
AE5
AE7
AH10
AA15
AH13
AH16
AH19
AH2
AH22
AH24
AH28
AH29
AH30
AH32
AH33
AH5
AH7
AJ7
AK10
AK7
AL12
AL14
AL15
AL17
AL18
AL2
AL20
AL21
AL23
AL24
AL26
AL28
AL30
AL32
AL33
AL5
AM13
AM16
AM19
AM22
AM25
AN1
AN10
AN13
AN16
AN19
AN22
AN25
AN30
AN34
AN4
AN7
AP2
AP33
B1
B10
B22
B25
B28
B31
B34
B4
B7
C10
C13
C19
C22
C25
C28
C7

GND_101
GND_102
GND_103
GND_104
GND_105
GND_106
GND_107
GND_108
GND_109
GND_110
GND_111
GND_112
GND_113
GND_114
GND_115
GND_116
GND_117
GND_118
GND_119
GND_120
GND_121
GND_122
GND_123
GND_124
GND_125
GND_126
GND_127
GND_128
GND_129
GND_130
GND_131
GND_132
GND_133
GND_134
GND_135
GND_136
GND_137
GND_138
GND_139
GND_140
GND_141
GND_142
GND_143
GND_144
GND_145
GND_146
GND_147
GND_148
GND_149
GND_150
GND_151
GND_152
GND_153
GND_154
GND_155
GND_156
GND_157
GND_158
GND_159
GND_160
GND_161
GND_162
GND_163
GND_164
GND_165
GND_166
GND_167
GND_168
GND_169
GND_170
GND_171
GND_172
GND_173
GND_174
GND_175
GND_176
GND_177
GND_178
GND_179
GND_180
GND_181
GND_182
GND_183
GND_184
GND_185
GND_186
GND_187
GND_188
GND_189
GND_190
GND_191
GND_192
GND_193
GND_194
GND_195
GND_196
GND_197
GND_198
GND_199
GND_200
GND_OPT_1
GND_OPT_2

D2
D31
E10
E22
E25
E5
E7
F28
G10
G13
G16
G19
G2
G22
G25
G28
G3
G30
G32
G33
G5
G7
K2
K28
K30
K32
K33
K6
K7
M13
M15
M17
M18
M20
M22
N12
N14
N16
N19
N2
N21
N23
N28
N30
N32
N33
N3
N5
P13
P15
P17
P18
P20
P22
R12
R14
R16
R19
R21
R23
T13
T15
T17
T18
T2
T20
T22
AG11
T28
T32
T5
T7
U12
U14
U16
U19
U21
U23
V12
V14
V16
V19
V21
V23
W13
W15
W17
W18
W20
W22
W28
Y12
Y14
Y16
Y19
Y21
Y23
AH11
C16
W32

+VGPU_CORE

C4400 EV@1U/6.3V 4
C4401 EV@1U/6.3V 4
C4402 EV@1U/6.3V 4
C4403 EV@1U/6.3V 4
C4404 EV@1U/6.3V 4
C4405 EV@1U/6.3V 4
C4406 EV@1U/6.3V 4
C4407 EV@1U/6.3V 4
C4408 EV@4.7U/6.3V 4
C4409 EV@4.7U/6.3V 4
C4410 EV@4.7U/6.3V 4
C4411 EV@4.7U/6.3V 4
C4412 EV@4.7U/6.3V 4

PLACE UNDER GPU

C4413 SP@4.7U/6.3V 4
C4414 EV@4.7U/6.3V 4
C4415 EV@4.7U/6.3V 4
C4416 EV@4.7U/6.3V 4

B2A

C4417 SP@4.7U/6.3V 4

B2A

C4418 EV@4.7U/6.3V 4

C4419 SP@4.7U/6.3V 4
C4420 EV@4.7U/6.3V 4

B2A

C4421 EV@4.7U/6.3V 4
C4422 EV@4.7U/6.3V 4

C4423 EV@10U/6.3V 4
C4814 EV@10U/6.3V 4
C4424 1 EV@22U/6.3V 6
C4425 1 EV@22U/6.3V 6
C4426 EV@10U/6.3V 4
C4813 EV@10U/6.3V 4
C4427 1 EV@22U/6.3V 6
C4428 1 EV@22U/6.3V 6

B2A

PLACE NEAR GPU

C4429 2 1 EV@22U/6.3V 6
C4430 EV@4.7U/6.3V 4
C4431 EV@4.7U/6.3V 4

C4432 EV@4.7U/6.3V 4

B2A

C4433 EV@4.7U/6.3V 4

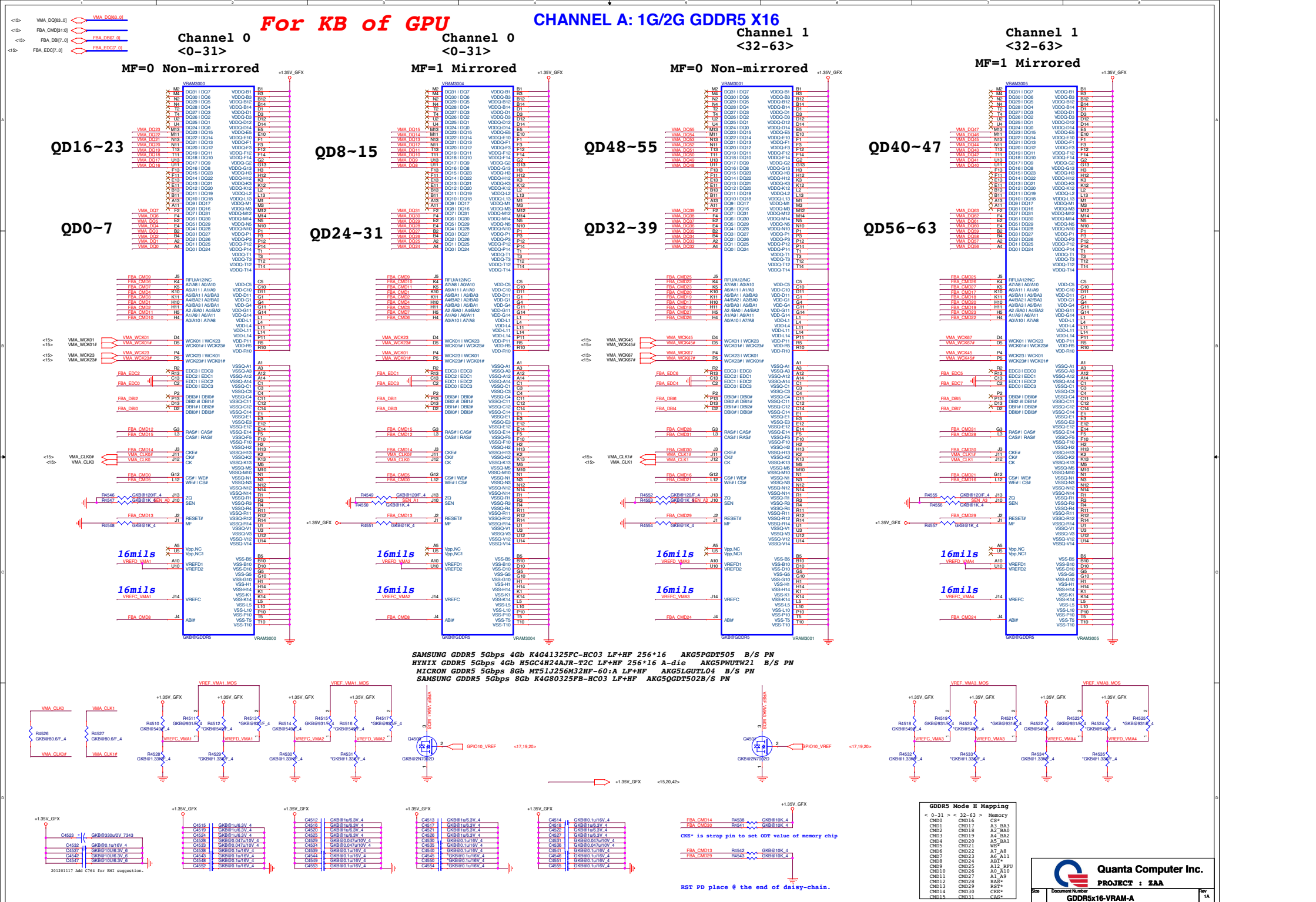
C4434 EV@4.7U/6.3V 4

C4435 330u/2V_7343

B2A

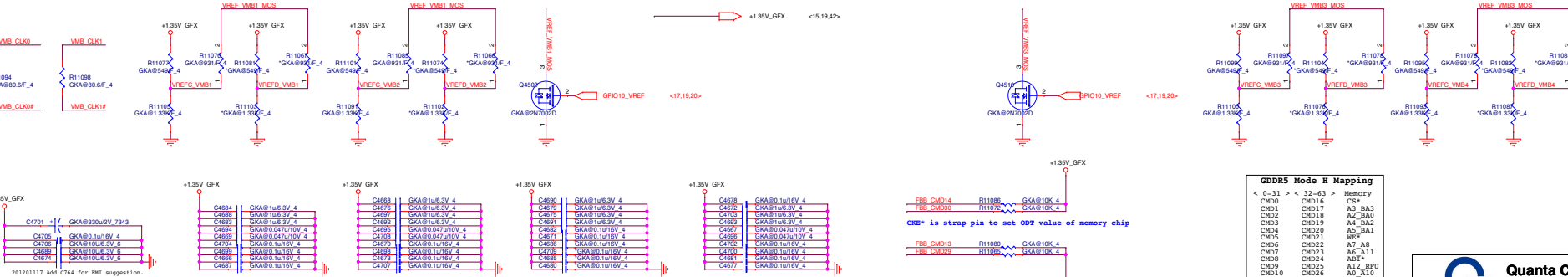



Quanta Computer Inc.
PROJECT : ZAA



Channel
<32-63>

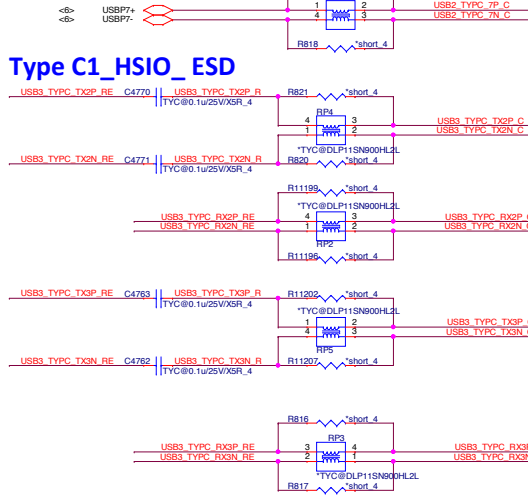
MF=1 Mirrored



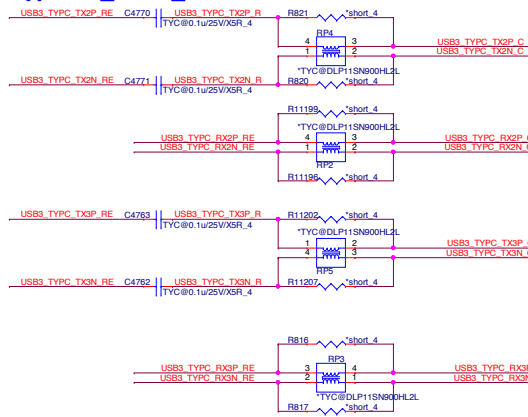
 Quanta Computer Inc. PROJECT : ZAA			
Size	Document Number	Rev	
	GDDR5x16-VRAM-B	1A	

USB TYPE-C

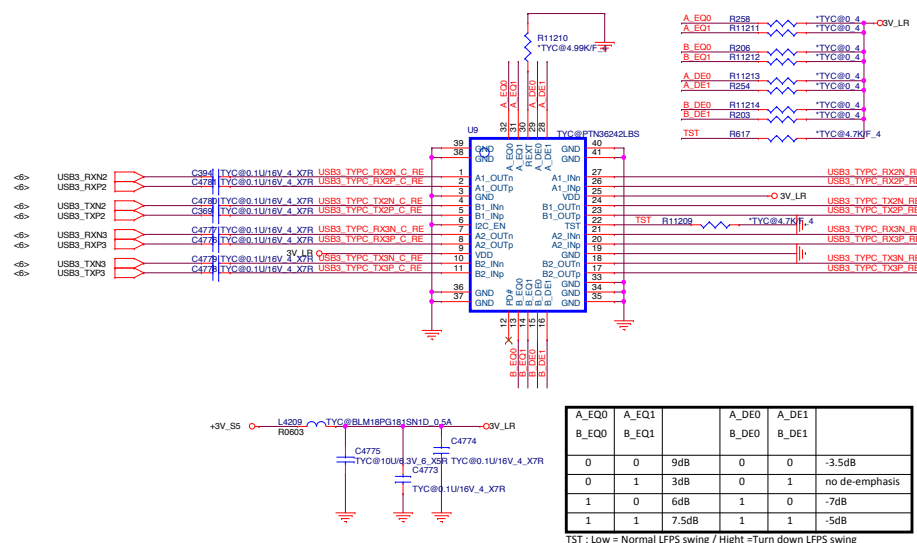
USB2.0 ESD



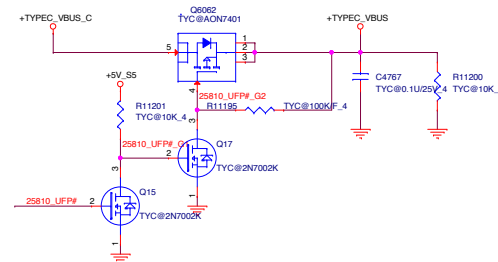
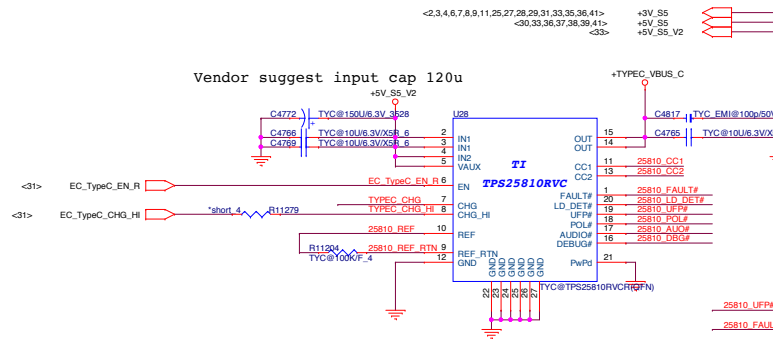
Type C1_HSIO_ESD



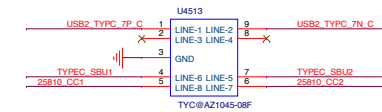
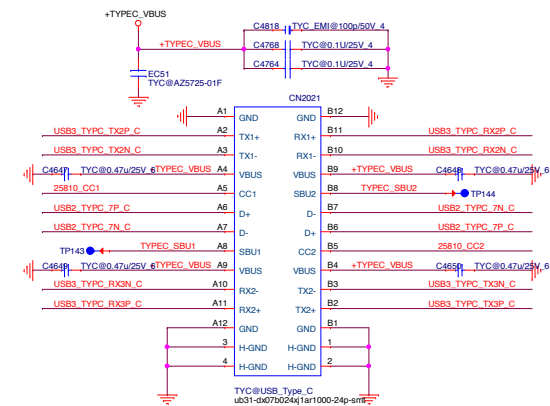
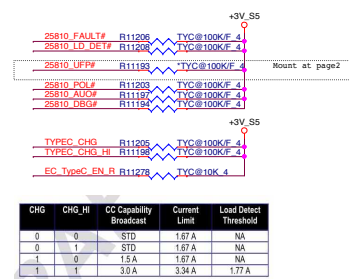
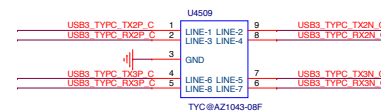
USB3 Re-Driver



Vendor suggest input cap 120u



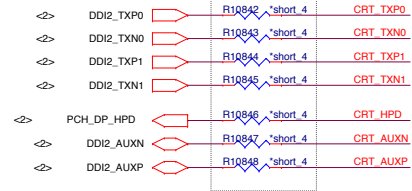
TPS25810 Port	CC1	CC2	OUT	VCONN On CC1 or CC2	POLs	UFPs	AUIOb	DEBUg
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	LOW	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z



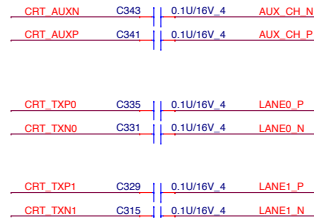
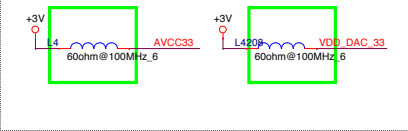
Quanta P/NAMAZING P/NUSD保護位置
BC104308Z00A21043-08F.R7G0.08TX RX (USB3.0 GEN1 5G)
BC104508Z00A21045-08F.R7G0.08D+ D- SBU1 SBU2 CC1 CC2
BC005725Z00A25725-01F.R7G0.009 PD 5V (follow 2AA)

DP TO VGA

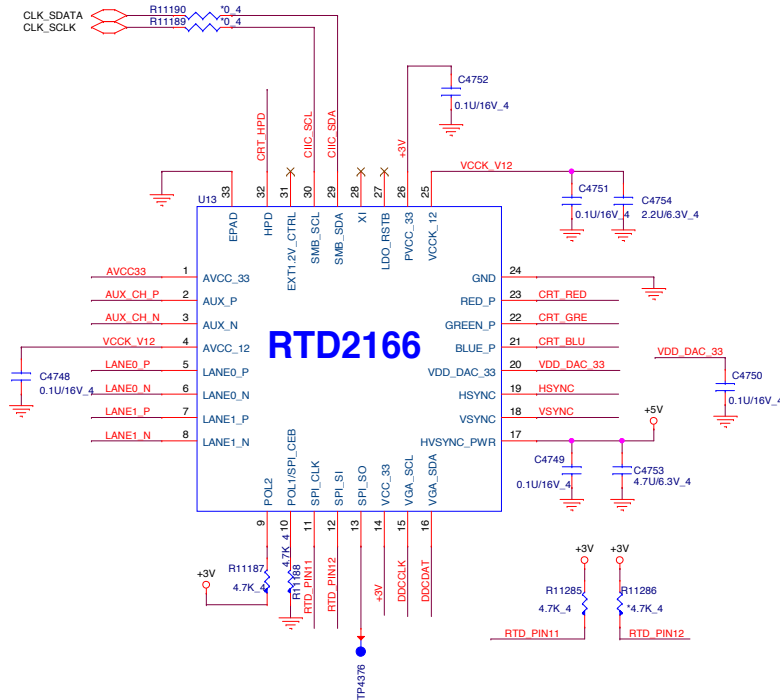
Close to CPU side of CAP.



Power



<7,12,13,28>
<7,12,13,29>

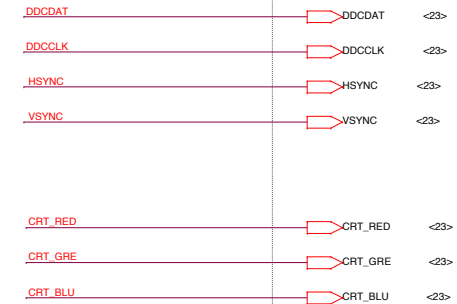


Note:

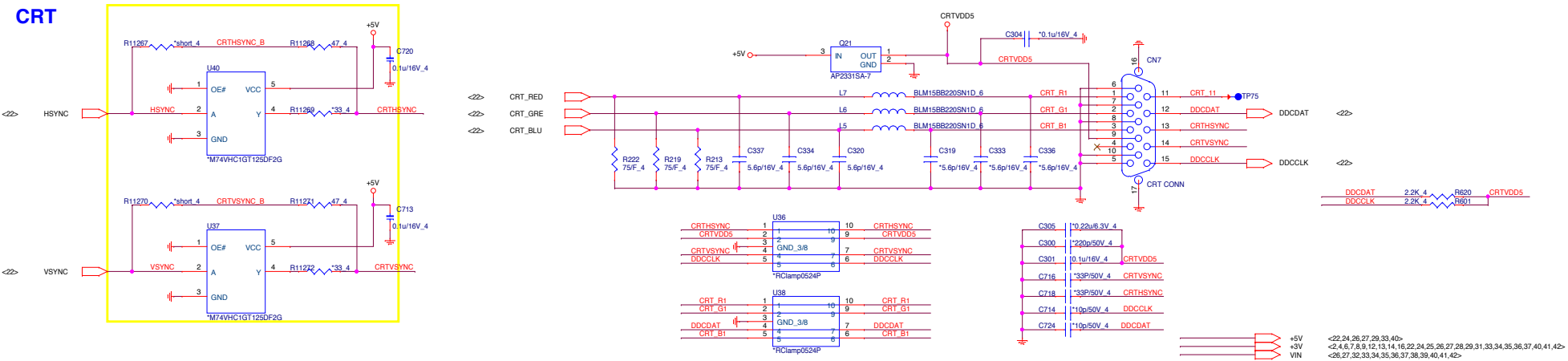
- 1- C1,C3,C4,C5,C11,C16, C21 should be placed close to chip
- 2- C5 should be X5R material
- 3- R6, R7, R8 should be 75 ohm with +/-1%
- 4- Suggest to connect Pin 29 and Pin 30 to PCH SMBUS for debug purpose.
- 5- This configuration is for internal ROM mode and using embedded LDO mode.



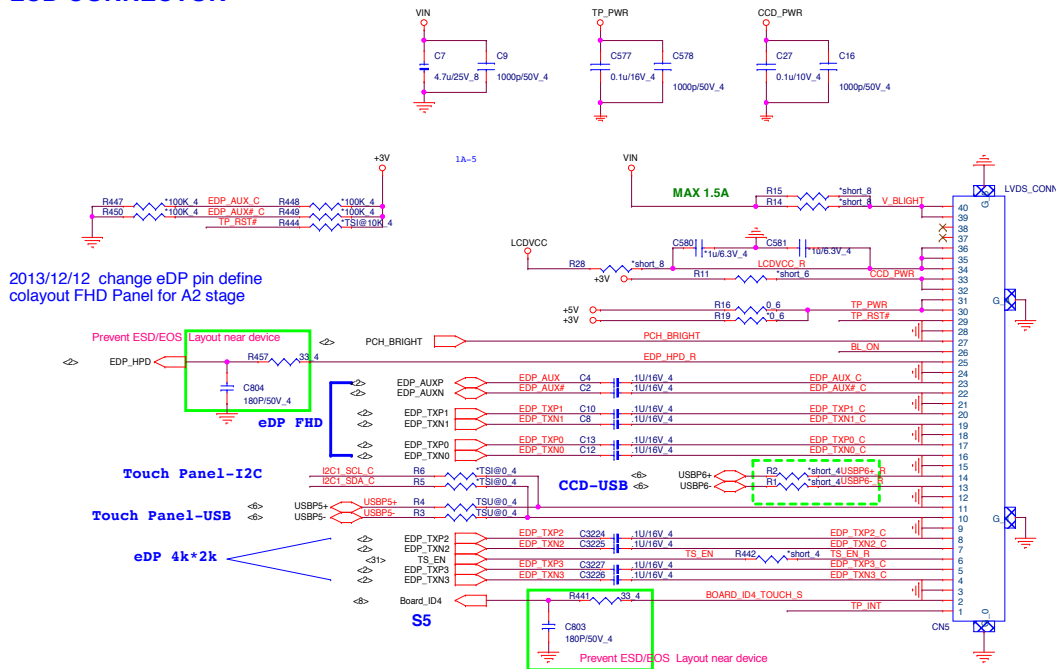
VGA



CRT



LCD CONNECTOR



2013/12/12 change eDP pin define
colayout FHD Panel for A2 stage

Touch Panel-I2C

Touch Panel-USB <6>

eDP 4k*2k \leq

1C1-2 2014/03/11 Add R698 for TS_EN short TP_INT,
for issue debug.

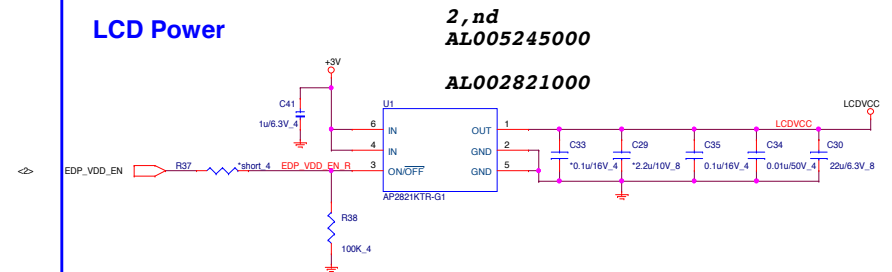
Touch Panel interrupt

Hall Sensor (HSR)

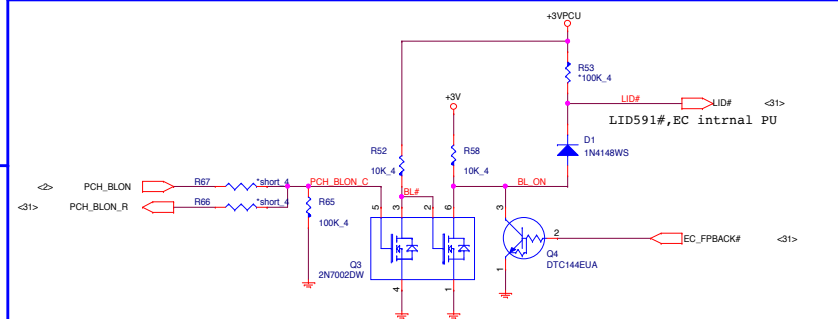
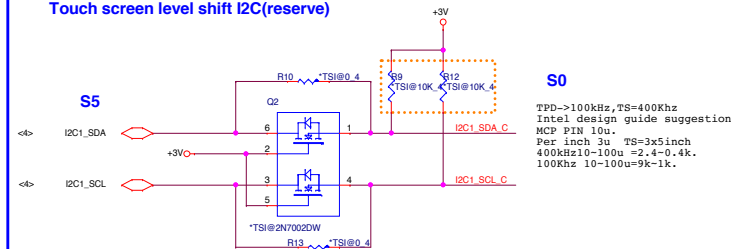
Rev:D
change to

```
AL009132001 (default)
AL008132004
AL008251000
```

LCD Power



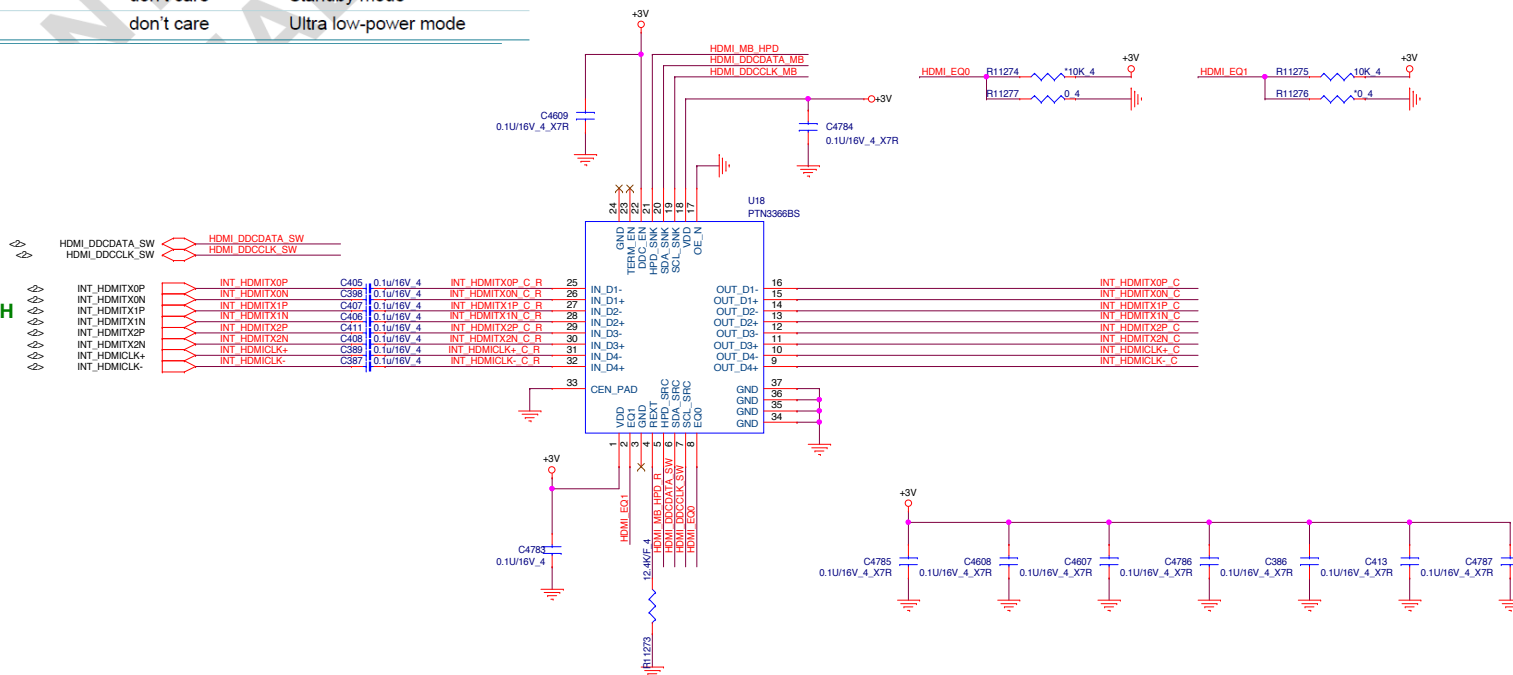
Touch screen level shift I2C(reserve)



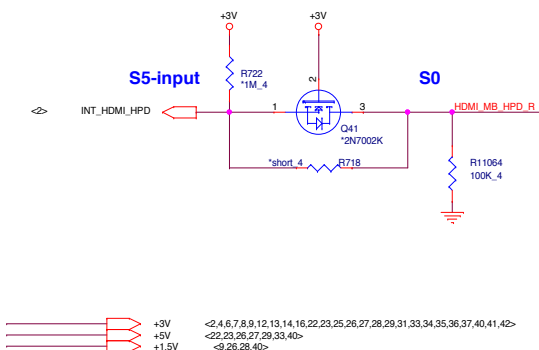
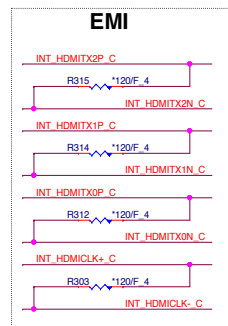
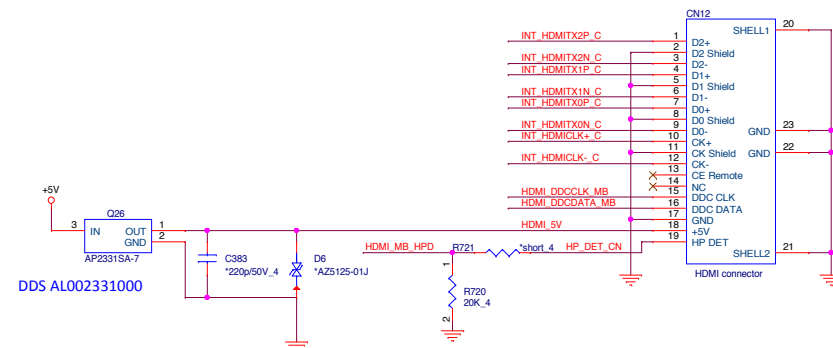
1B-3 2013/12/10 change Q3.3 from +3V to +3VPCU.

OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode

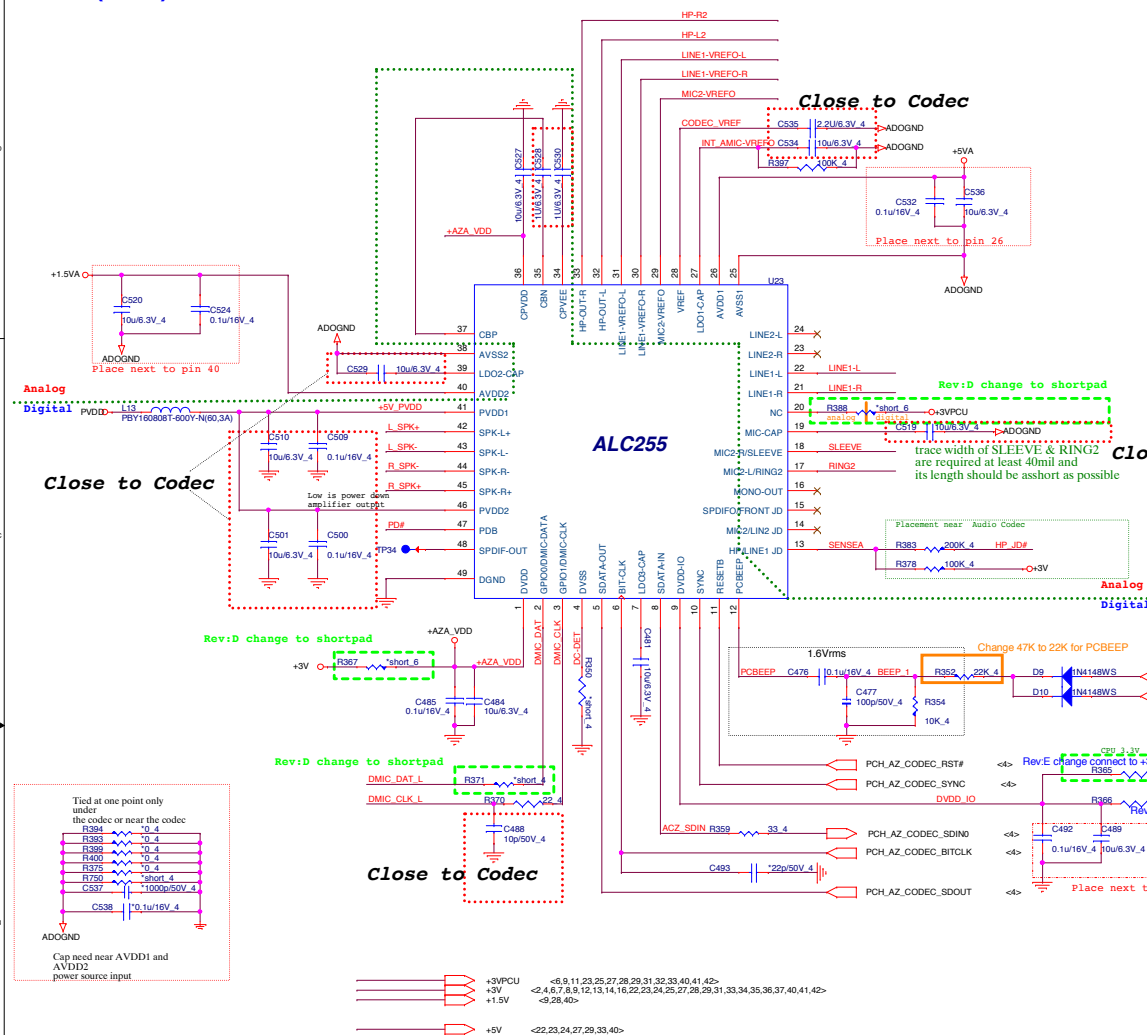
From PCH



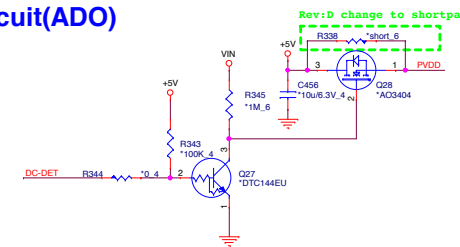
HDMI connector



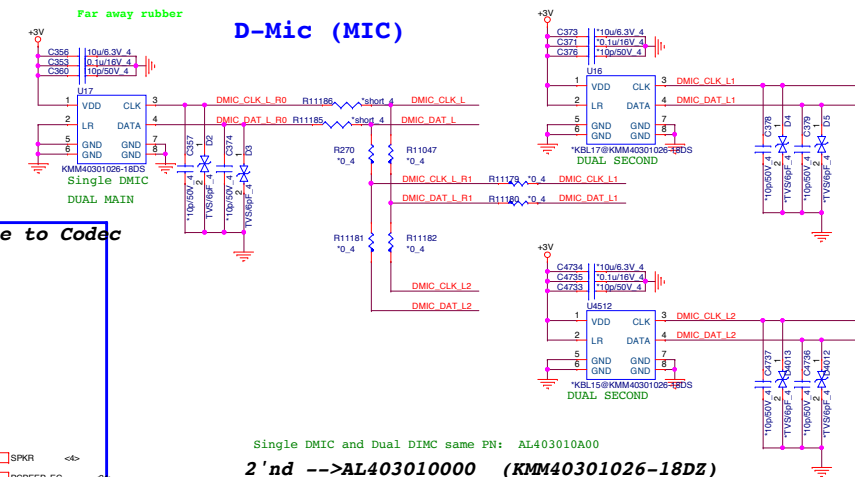
Codec(ADO)



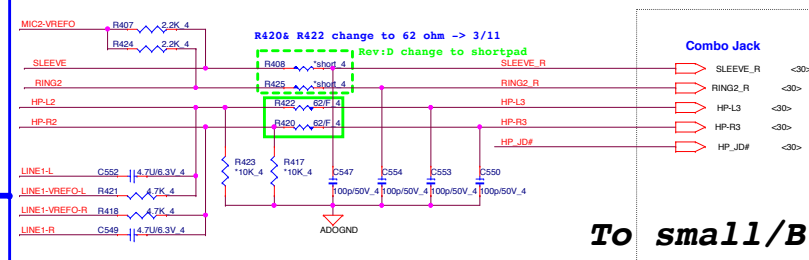
DC-DET circuit(ADO)



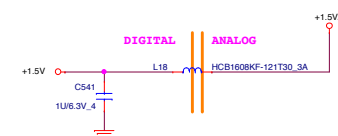
D-Mic (MIC)



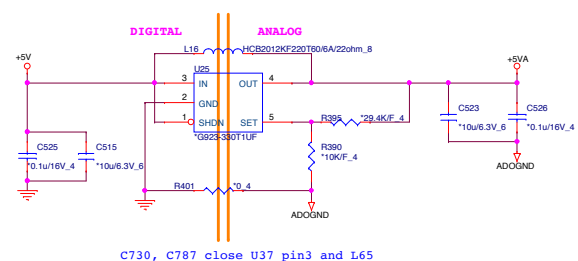
Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)



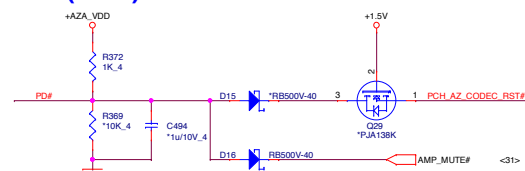
Codec PWR 1.5V(ADO)



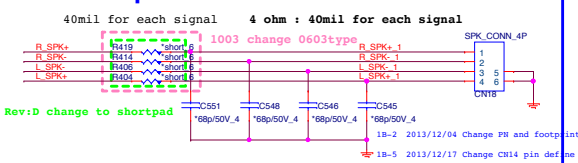
Codec PWR 5V(ADO)



Mute(ADO)

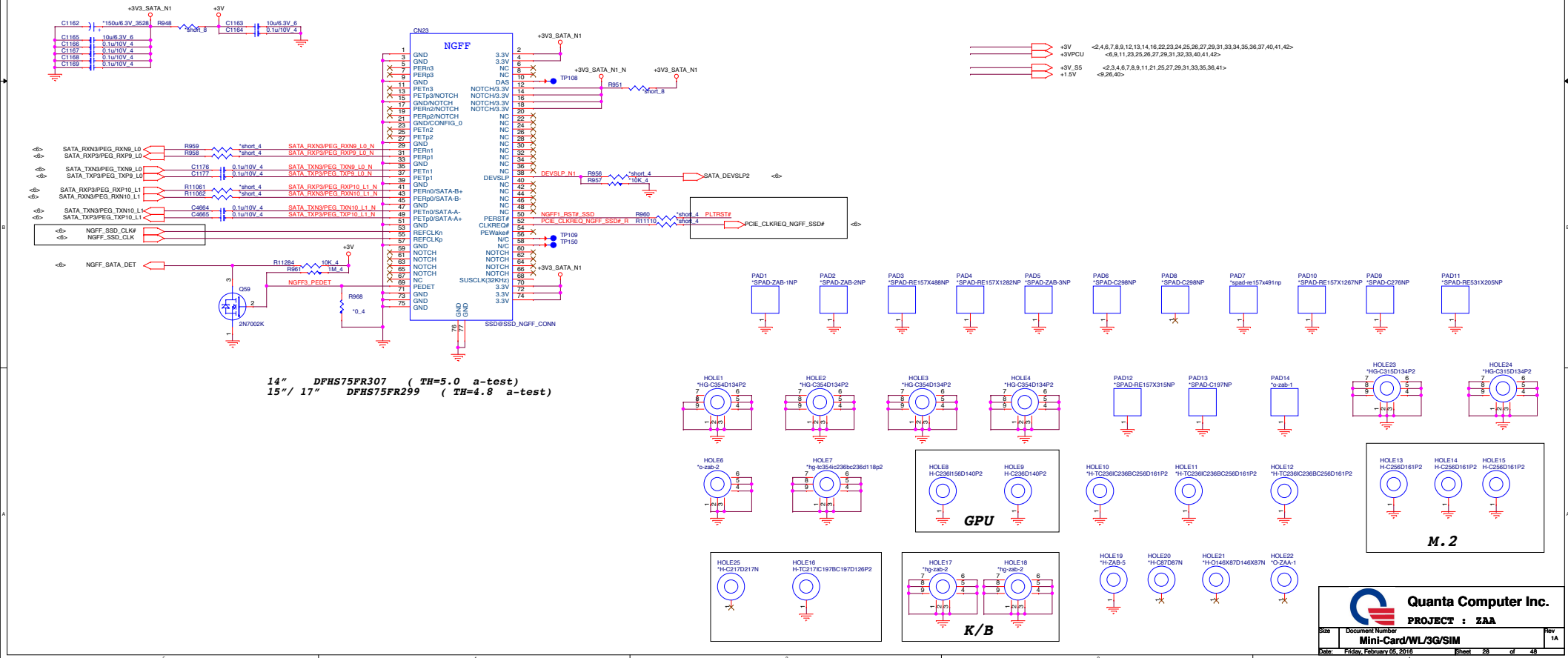
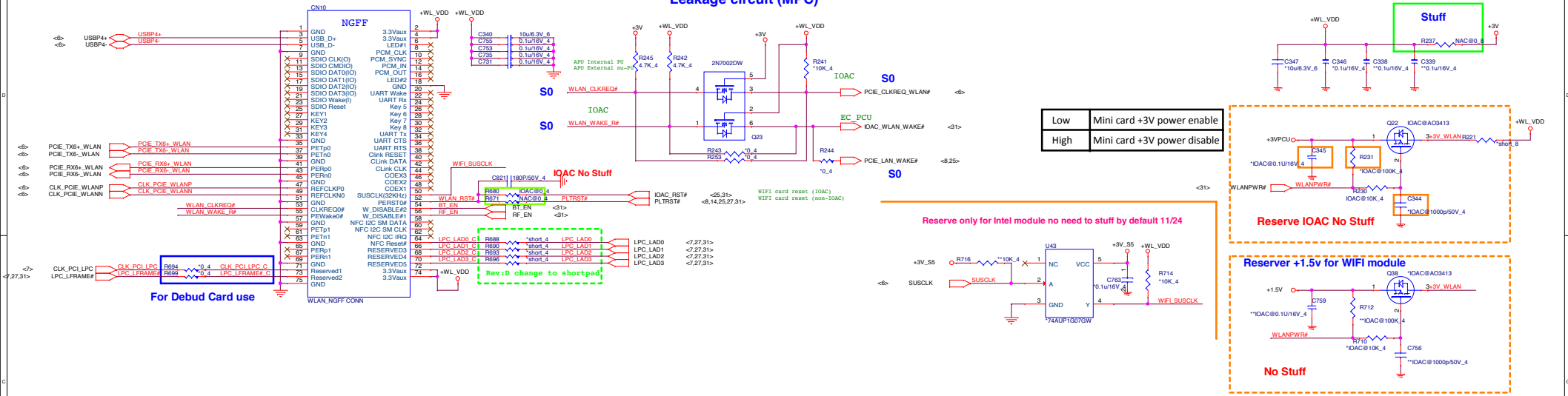


Internal Speaker

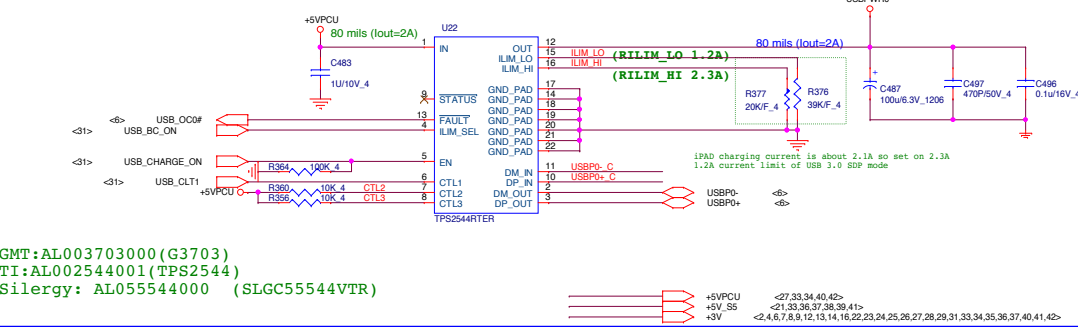


NGFF_M.2 WIFI & BT (NGF)

Leakage circuit (MPC)



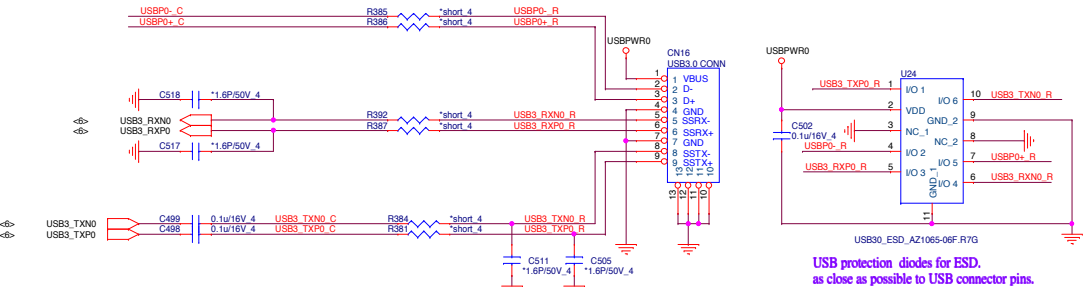
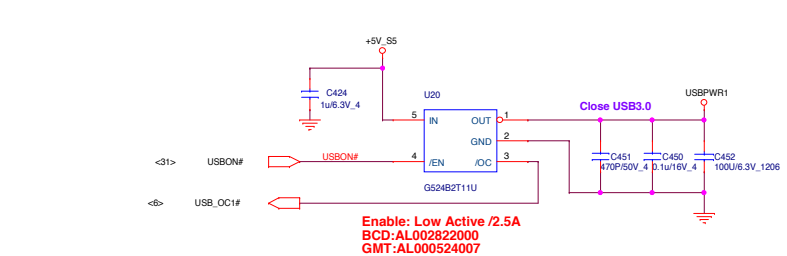
USB Charger to 3.0 (UBC)



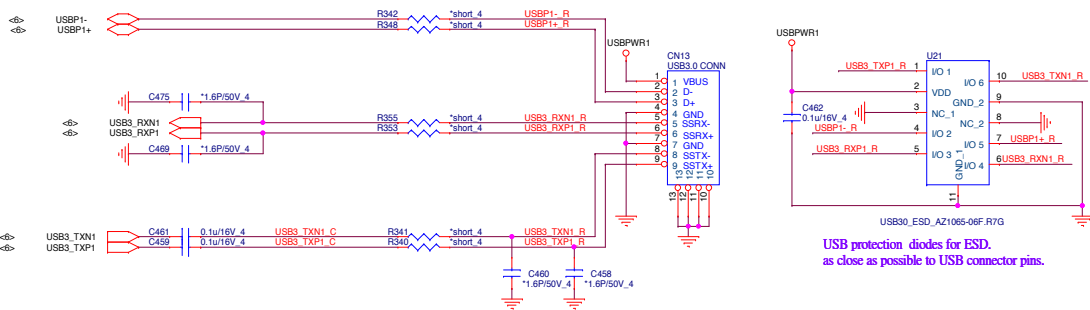
	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

RILIM LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1) $I_{OS_typ}(mA) = 50,250 / (RILIM_XX(K\Omega) + 0.1)$
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

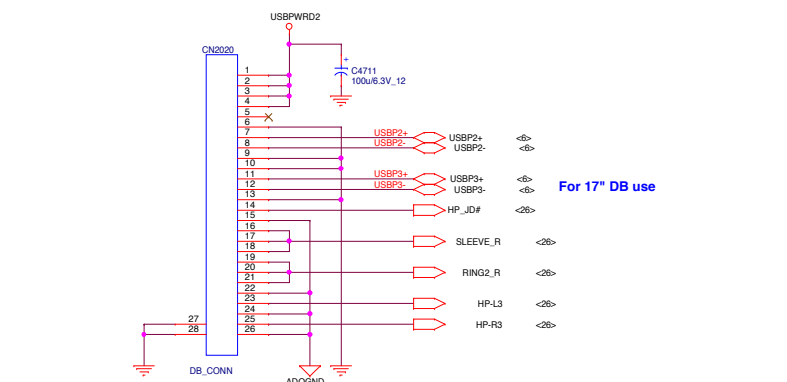
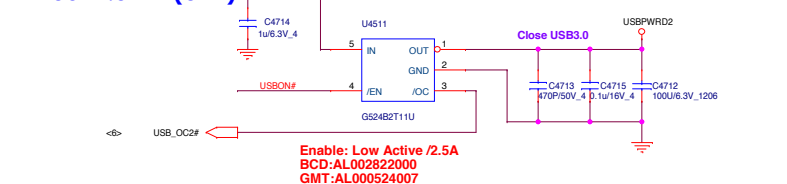
USB 3.0 Connector (UB3)

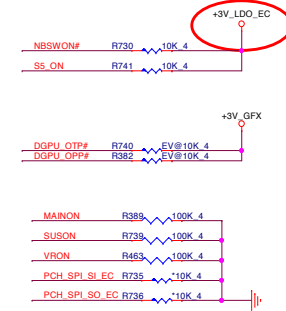
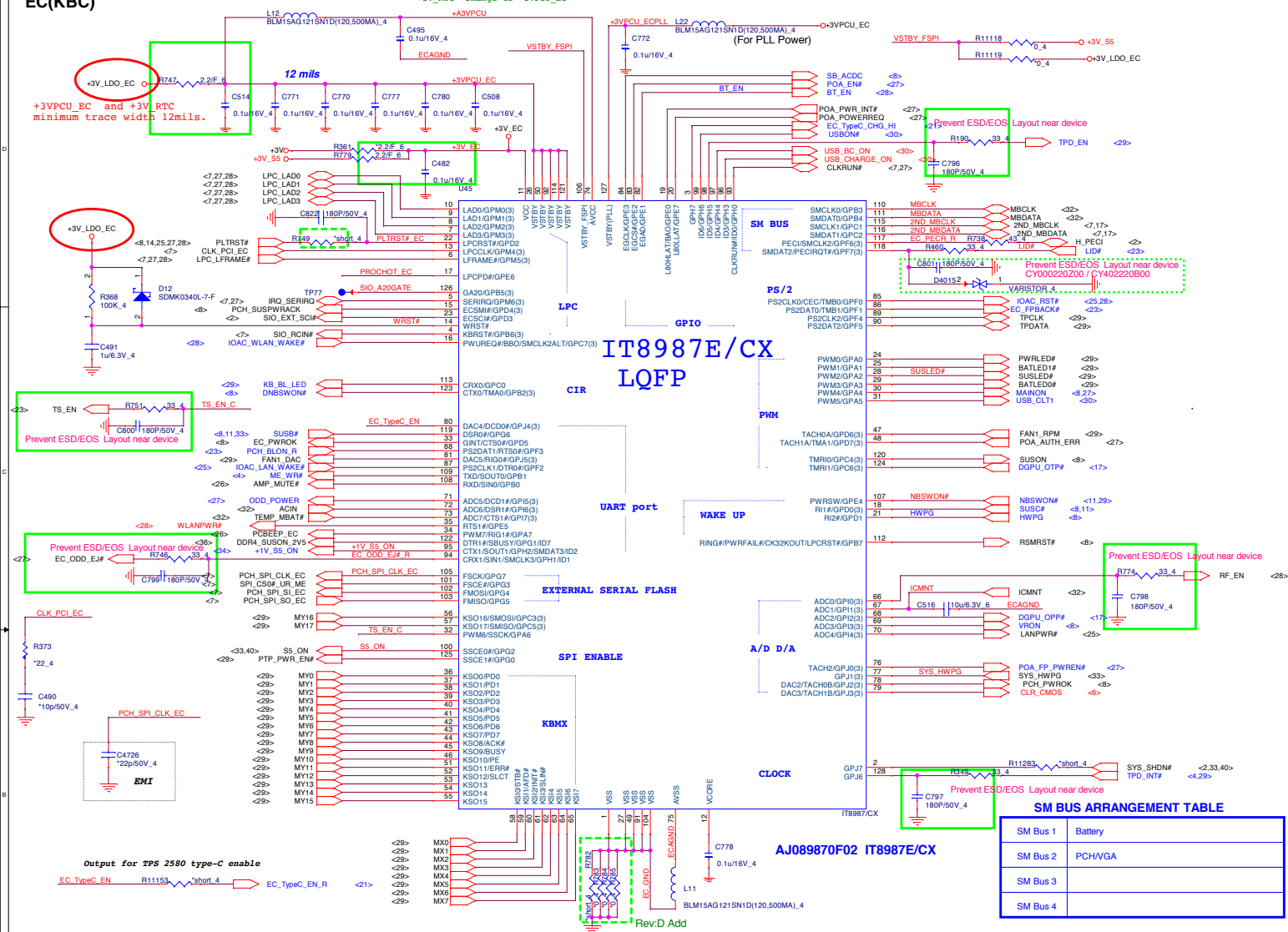


USB3.0 conn, 2'nd : DFHS09FR679

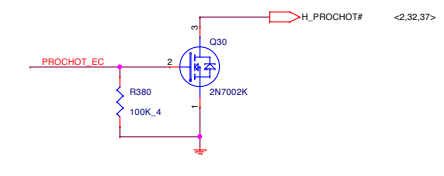
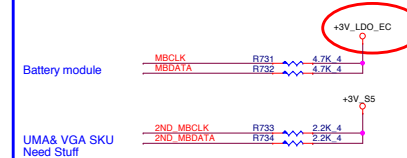


USB2.0 DB (UB2)



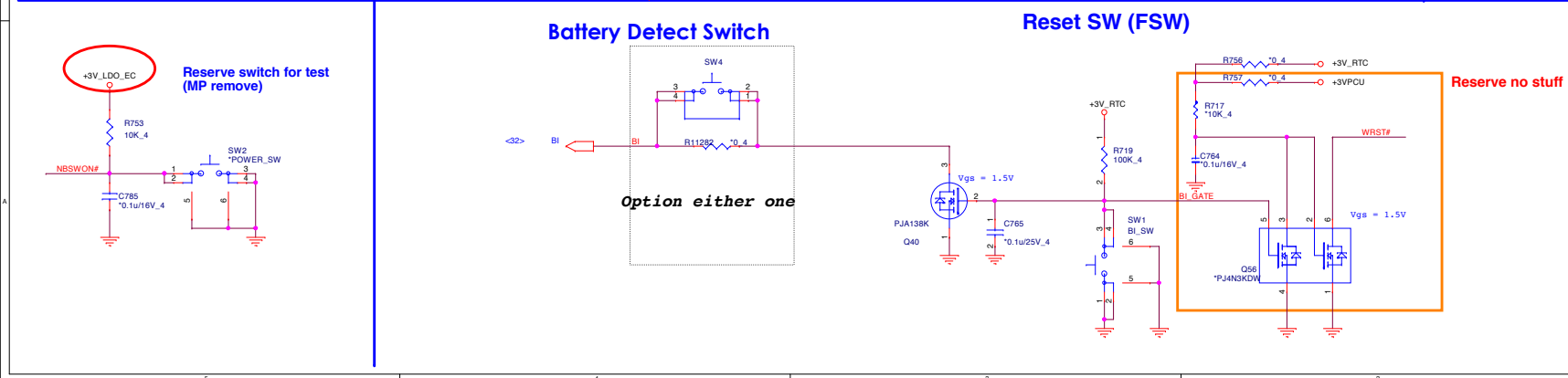
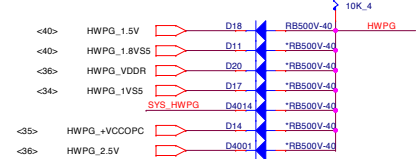


SM BUS PU(KBC)

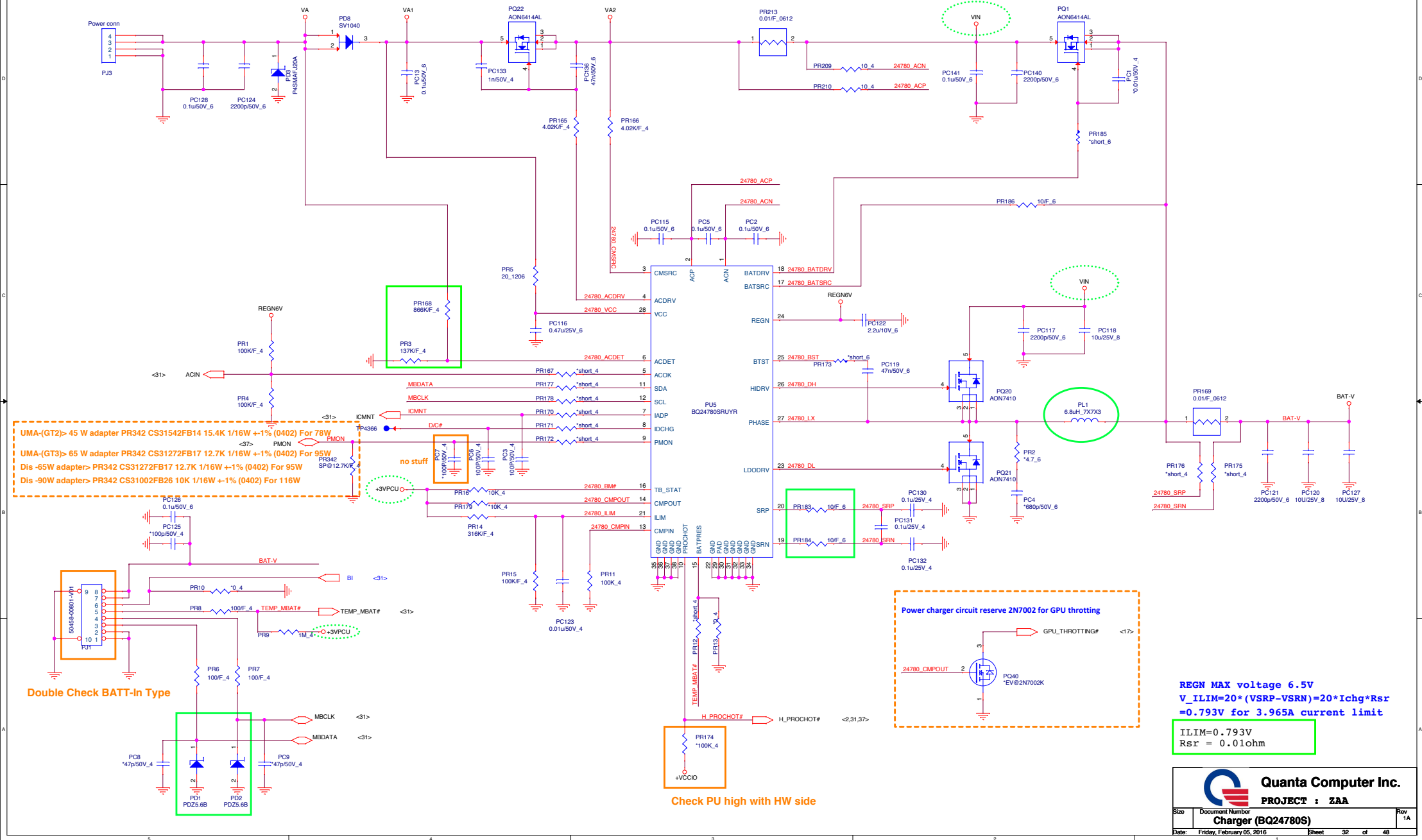


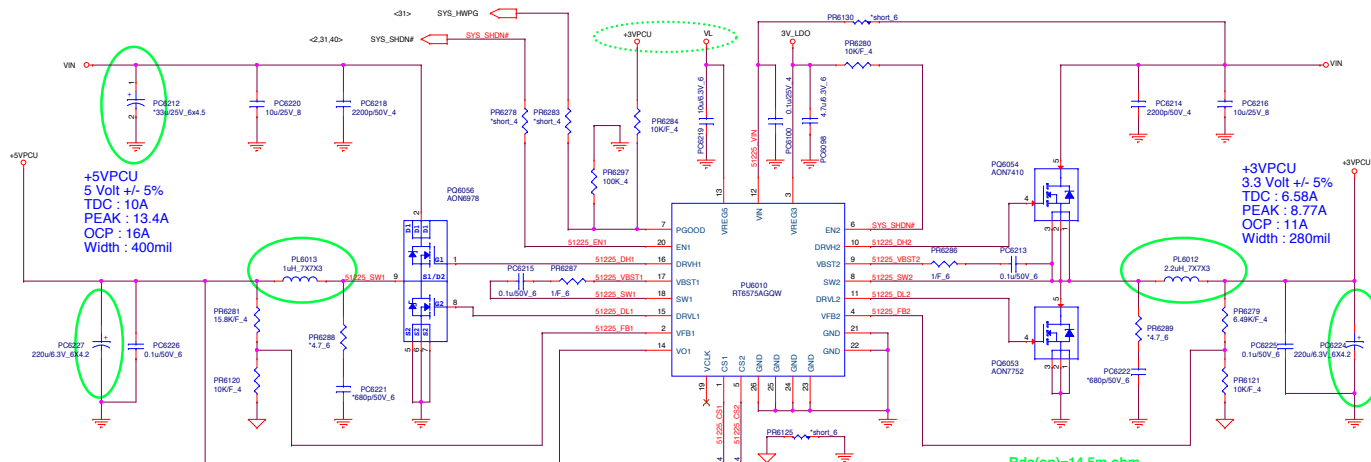
HWPG(KBC)

DDR=1.5V, D1 DNP and D2 POP
DDR=1.35V, D1 POP and D2 DNP



Double Check ADP-In Type





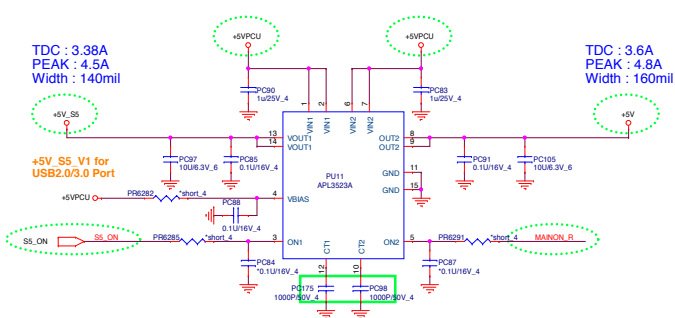
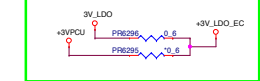
OCP:16A
 $L(\text{ripple current}) = (9.3) \cdot 3.3 / (2.2 \cdot 0.355 \text{M}^9) = 7.407\text{A}$
 $I_{\text{ocp}} = 18 - (7.407/2) = 12.296\text{A}$
 $V_{\text{th}} = (12.296\text{A} \cdot 4.5\text{mOhm}) + 1\text{mV} = 61.252\text{mV}$
 $R(\text{lim}) = (61.252\text{mV}^8) / 10\text{uA} \sim 49\text{K}$

Rds(on)=4.9m ohm

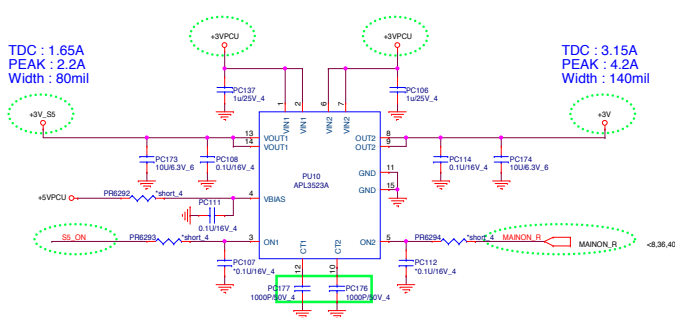
OCP:11A
 $L(\text{ripple current}) = (9.3) \cdot 3.3 / (2.2 \cdot 0.355 \text{M}^9) \sim 2.676\text{A}$
 $I_{\text{ocp}} = 11 - (2.676/2) = 9.662\text{A}$
 $V_{\text{th}} = (9.662\text{A} \cdot 14.5\text{mOhm}) + 1\text{mV} = 141.099\text{mV}$
 $R(\text{lim}) = (141.099\text{mV}^8) / 10\text{uA} \sim 112.68\text{K}$

Rds(on)=14.5m ohm

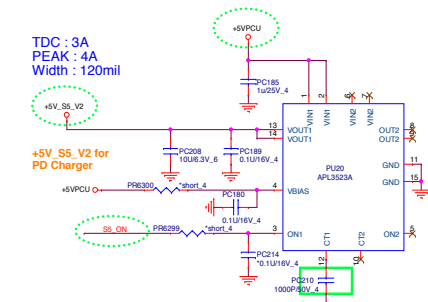
Power auto recovery



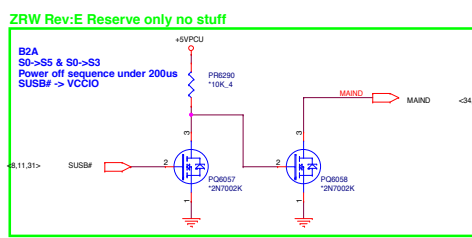
Soft-Start

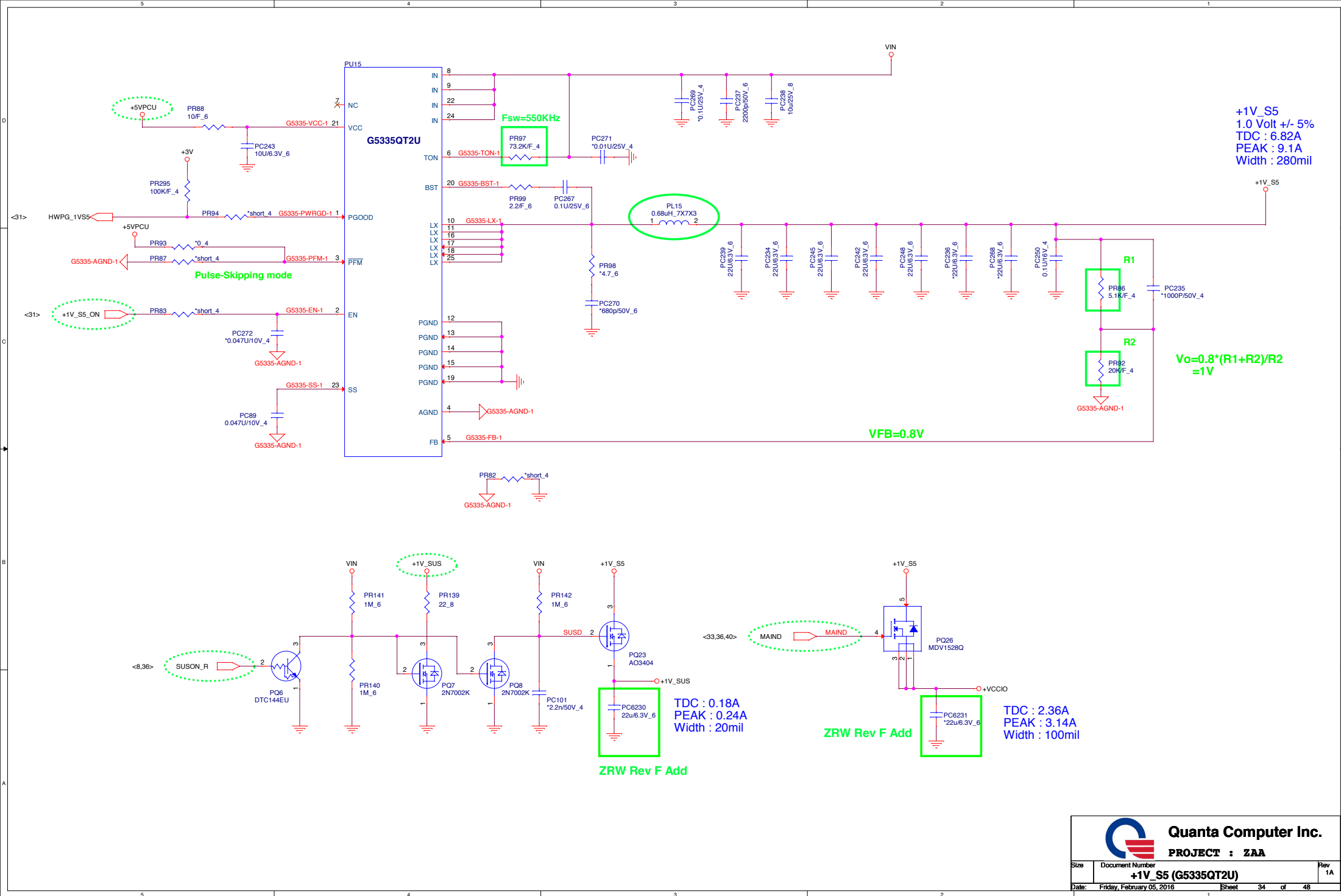


Soft-Start



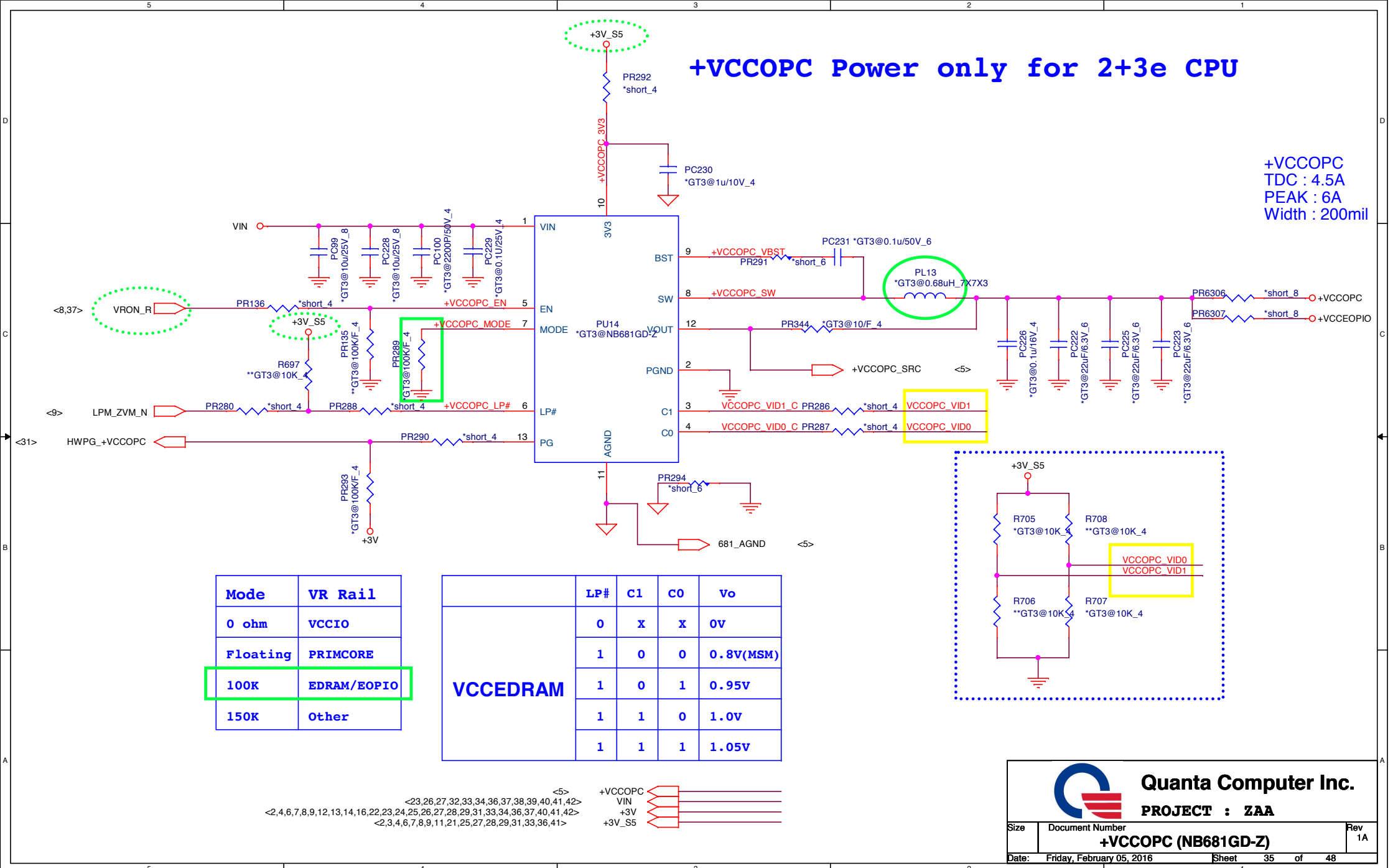
Soft-Start





+VCCOPC Power only for 2+3e CPU

+VCCOPC
TDC : 4.5A
PEAK : 6A
Width : 200mil



Check PU high with HW

SVID near PU1

ZRW REV-F add 1000p

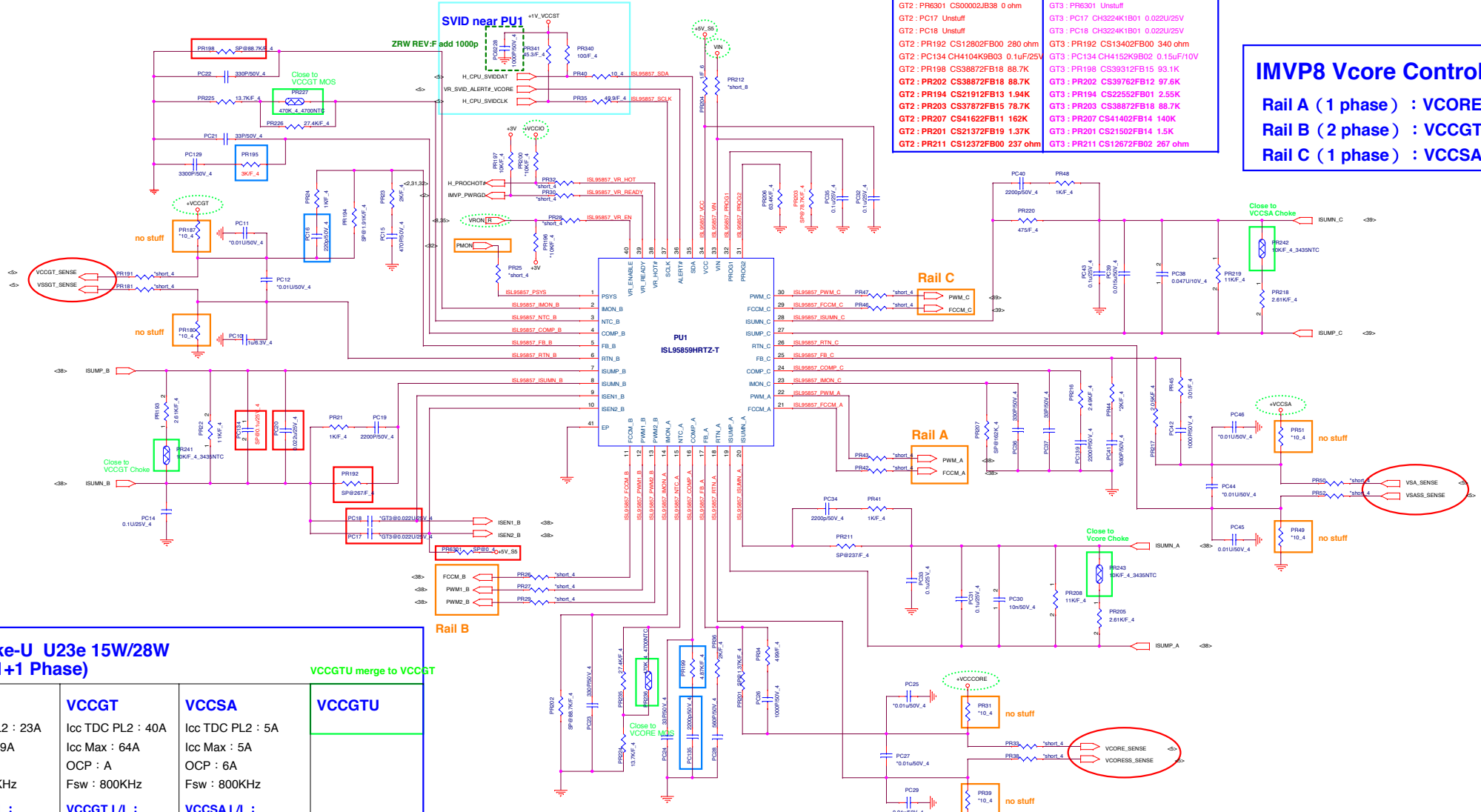
IMVP8 Vcore Controller

Rail A (1 phase) : VCORE

Rail B (2 phase) : VCCGT

Rail C (1 phase) : VCCSA

GT2 : PR19 Unstuff	GT3 : PR19 CS4100F932 100K
GT2 : PR6301 CS00002JB38 0 ohm	GT3 : PR6301 Unstuff
GT2 : PC17 Unstuff	GT3 : PC17 CH3224K1B01 0.022U/25V
GT2 : PC18 Unstuff	GT3 : PC18 CH3224K1B01 0.022U/25V
GT2 : PR192 CS12802FB00 280 ohm	GT3 : PR192 CS13402FB00 340 ohm
GT2 : PC134 CH4104K9B03 0.1uF/25V	GT3 : PC134 CH4152K9B02 0.15uF/10V
GT2 : PR198 CS38872FB18 88.7K	GT3 : PR198 CS39312FB15 93.1K
GT2 : PR202 CS38872FB18 88.7K	GT3 : PR202 CS39762FB12 97.6K
GT2 : PR194 CS21912FB13 1.94K	GT3 : PR194 CS22552FB01 2.55K
GT2 : PR203 CS37872FB15 78.7K	GT3 : PR203 CS38872FB18 88.7K
GT2 : PR207 CS41622FB11 162K	GT3 : PR207 CS41402FB14 140K
GT2 : PR201 CS21372FB19 1.37K	GT3 : PR201 CS21502FB14 1.5K
GT2 : PR211 CS12372FB02 237 ohm	GT3 : PR211 CS12672FB02 267 ohm



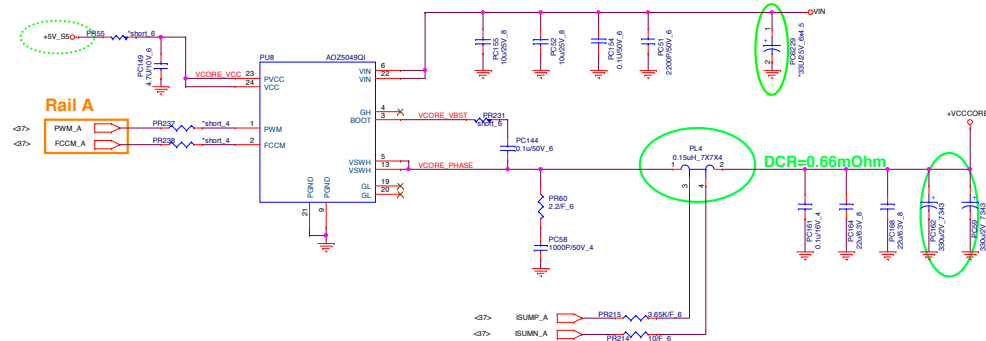
Skylake-U U23e 15W/28W (1+2+1 Phase)

VCORE	VCCGT	VCCSA	VCCGTU
Icc TDC PL2 : 23A	Icc TDC PL2 : 40A	Icc TDC PL2 : 5A	
Icc Max : 29A	Icc Max : 64A	Icc Max : 5A	
OCF : 35A	OCF : A	OCF : 6A	
Fsw : 800KHz	Fsw : 800KHz	Fsw : 800KHz	
VCORE L/L :	VCCGT L/L :	VCCSA L/L :	
R_DC_LL : 2.1mV/A	R_DC_LL : 2mV/A	R_DC_LL : 10.3mV/A	
R_AC_LL : 2.1mV/A	R_AC_LL : 2mV/A	R_AC_LL : 10.3mV/A	

VCORE

VCORE 1/4 :

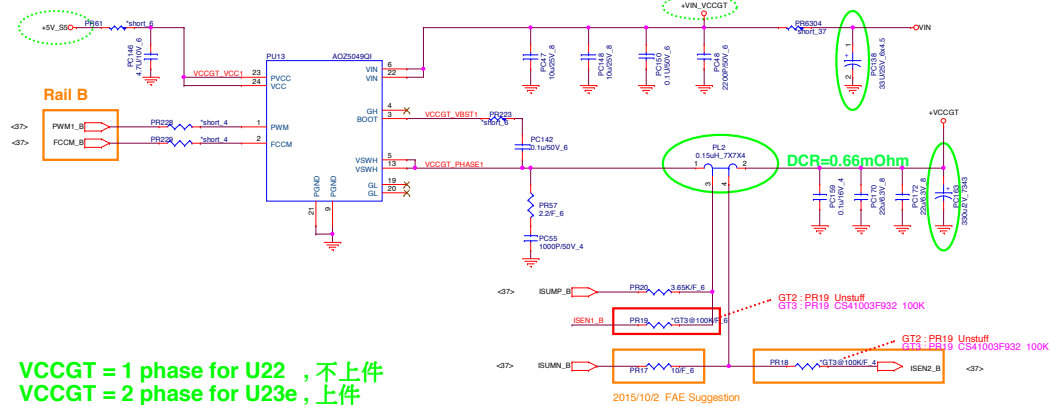
R_AC_LL : 2.1mV/A



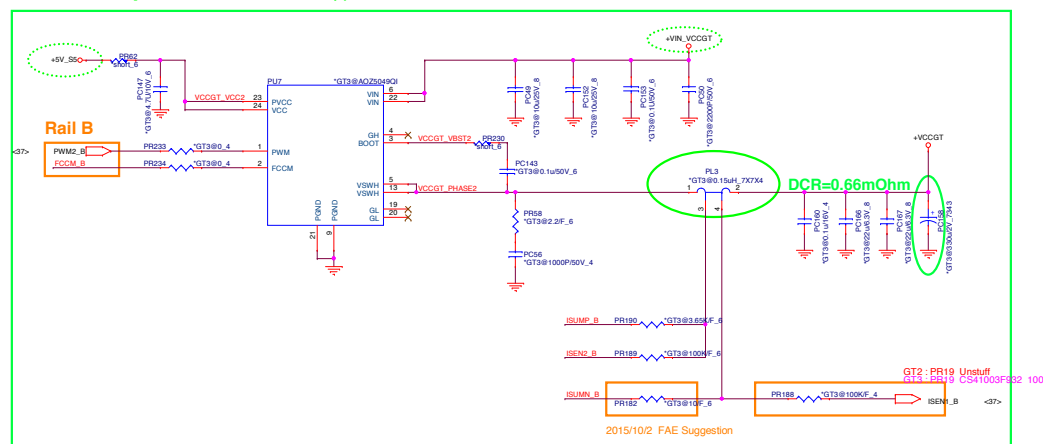
VCCGT

Fsw : 800KHz

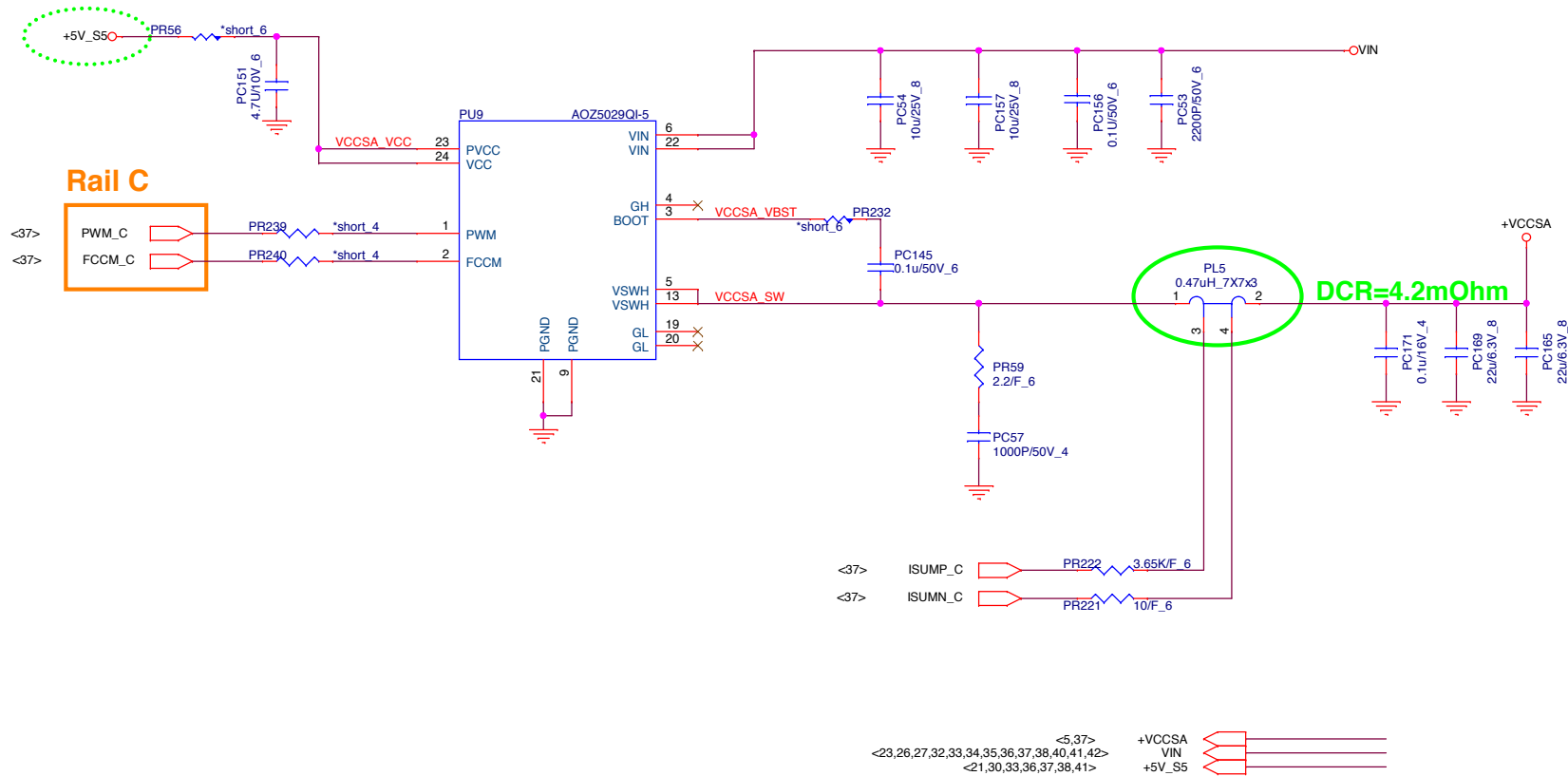
R_AC_LL : 2mV/A



VCCGT = 1 phase for U22 , 不上件
VCCGT = 2 phase for U23e , 上件



VCCSA



VCCSA

Icc TDC PL2 : 5A

Icc Max : 5A

OCP : 6A

Fsw : 800KHz

VCCSA L/L :

R_DC_LL : 10.3mV/A

R_AC_LL : 10.3mV/A

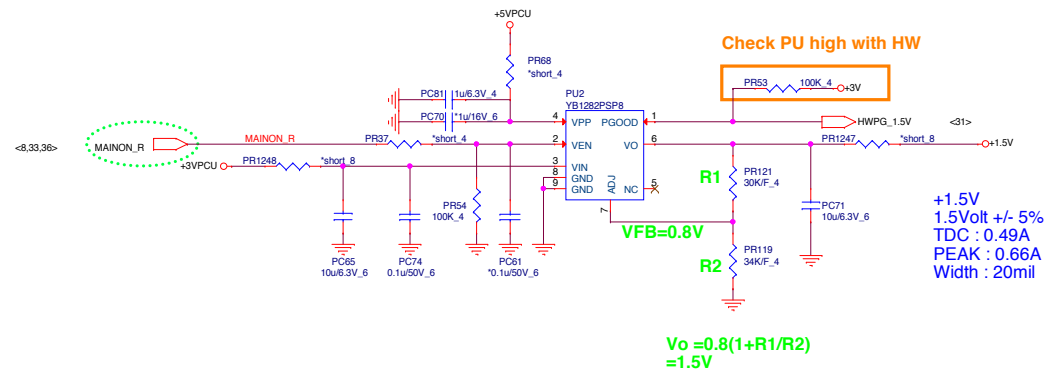
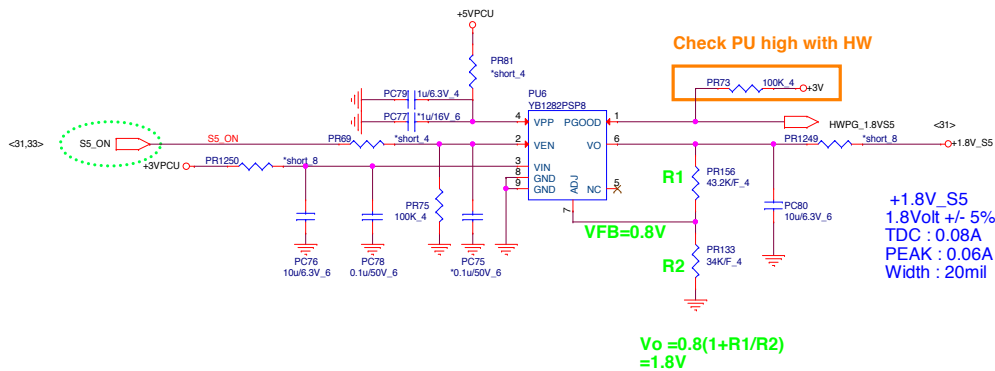


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PROJECT : ZAA

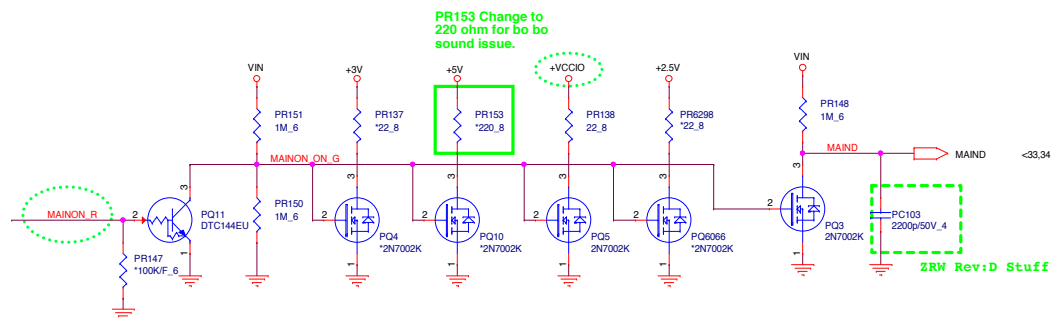
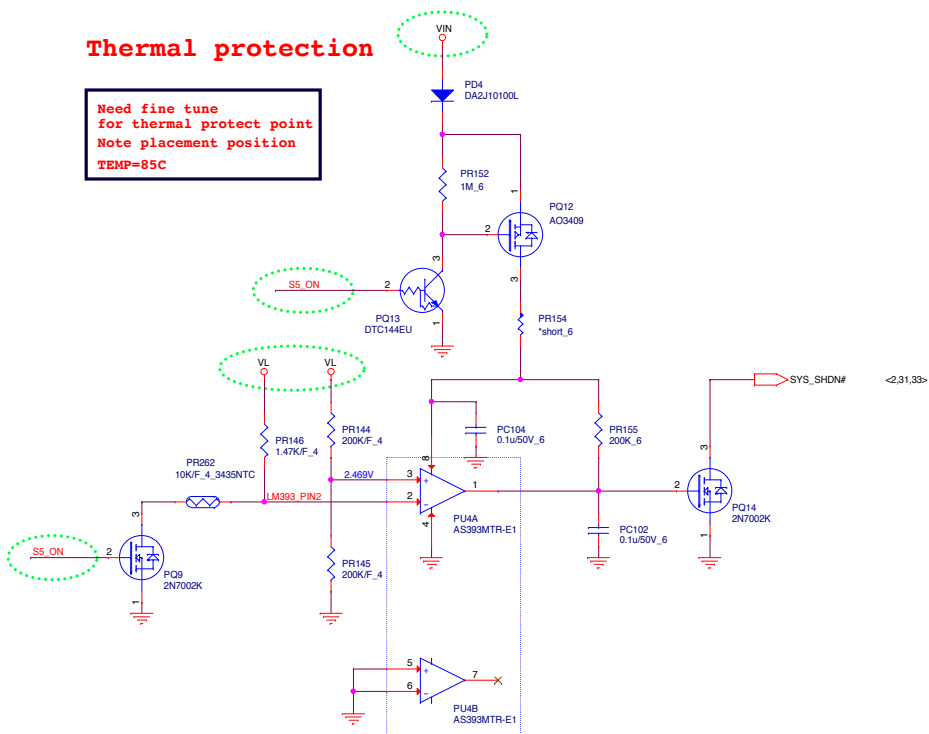
Size	Document Number	Rev
	VCCSA (ISL95808HRZ-T)	1A

Date: Friday, February 05, 2016 Sheet 39 of 48



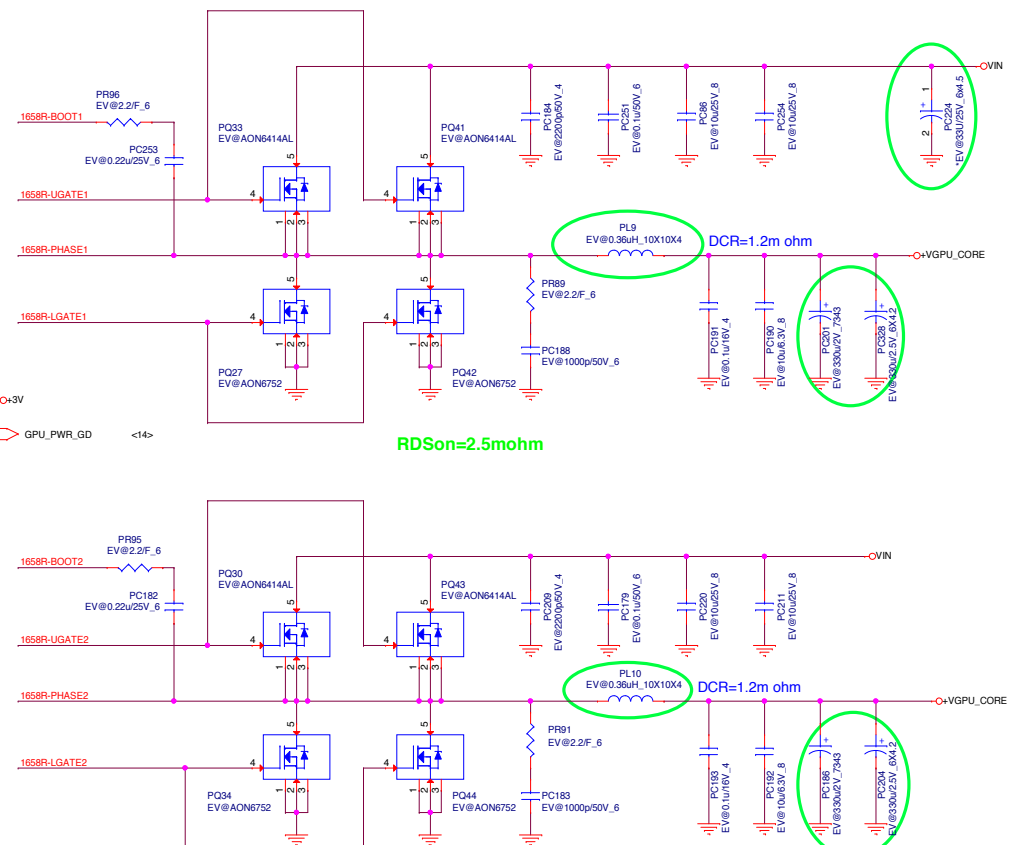
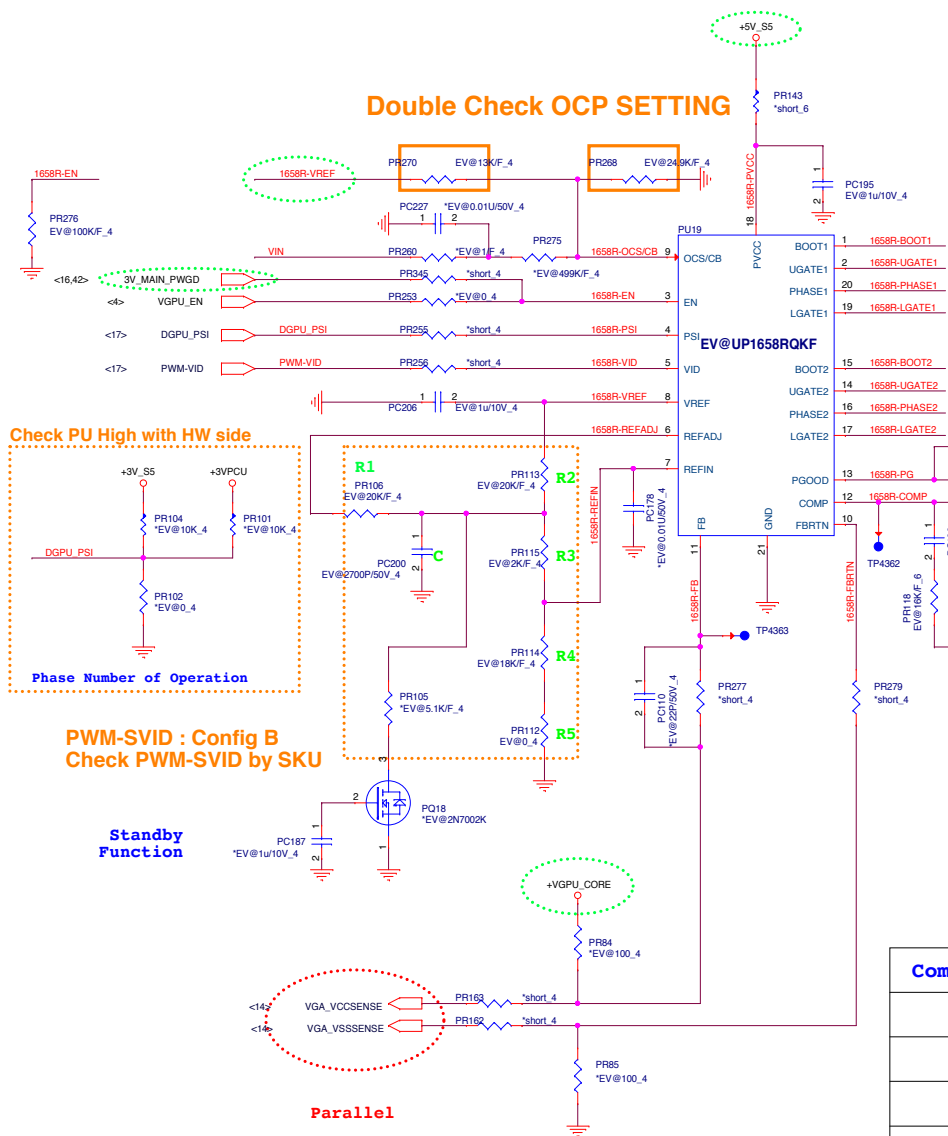
Thermal protection

Need fine tune
for thermal protect point
Note placement position
TEMP=85C



Quanta Computer Inc.
PROJECT : ZAA

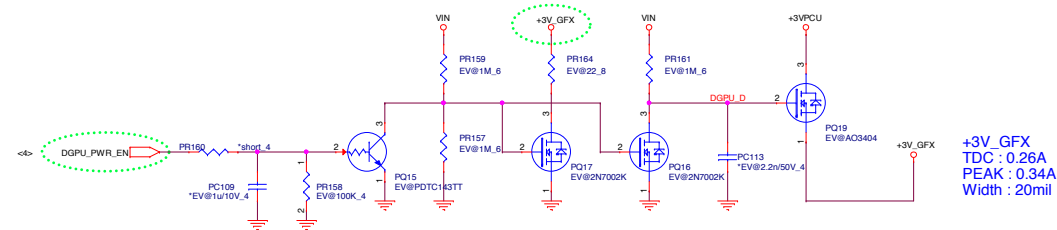
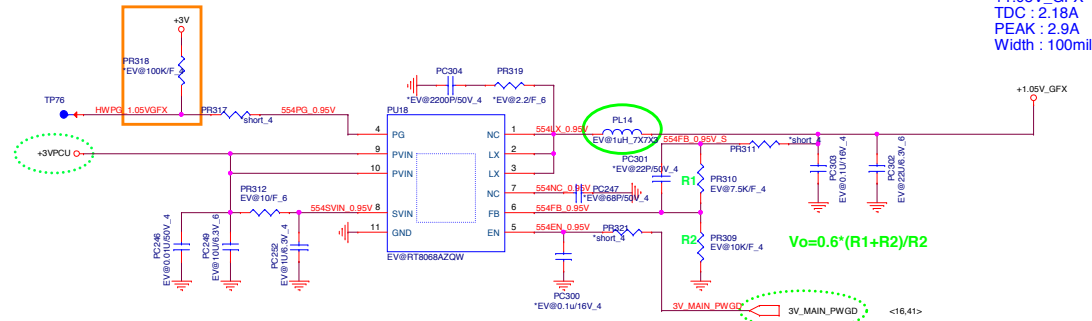
Size	Document Number	Rev
	+1.8V/+1.5V/Thermal Protect	1A
Date:	Friday, February 05, 2016	Sheet 40 of 48



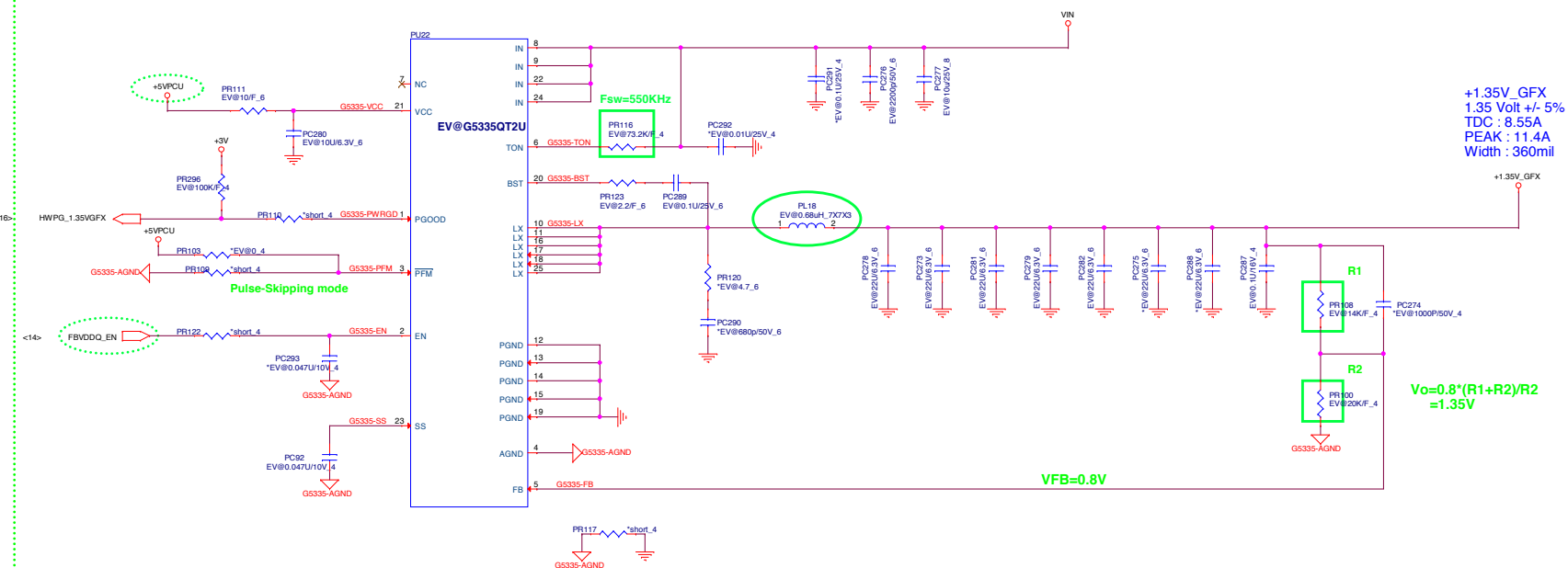
Component Value	Config B
R1	20K
R2	20K
R3	2K
R4	18K
R5	0-ohm
C	2.7nF

```
+VGPU_CORE
Countinue current:51.1A
Peak current:87A
OCP:112A
FSW:300KHz
L/L=0mV/A
```

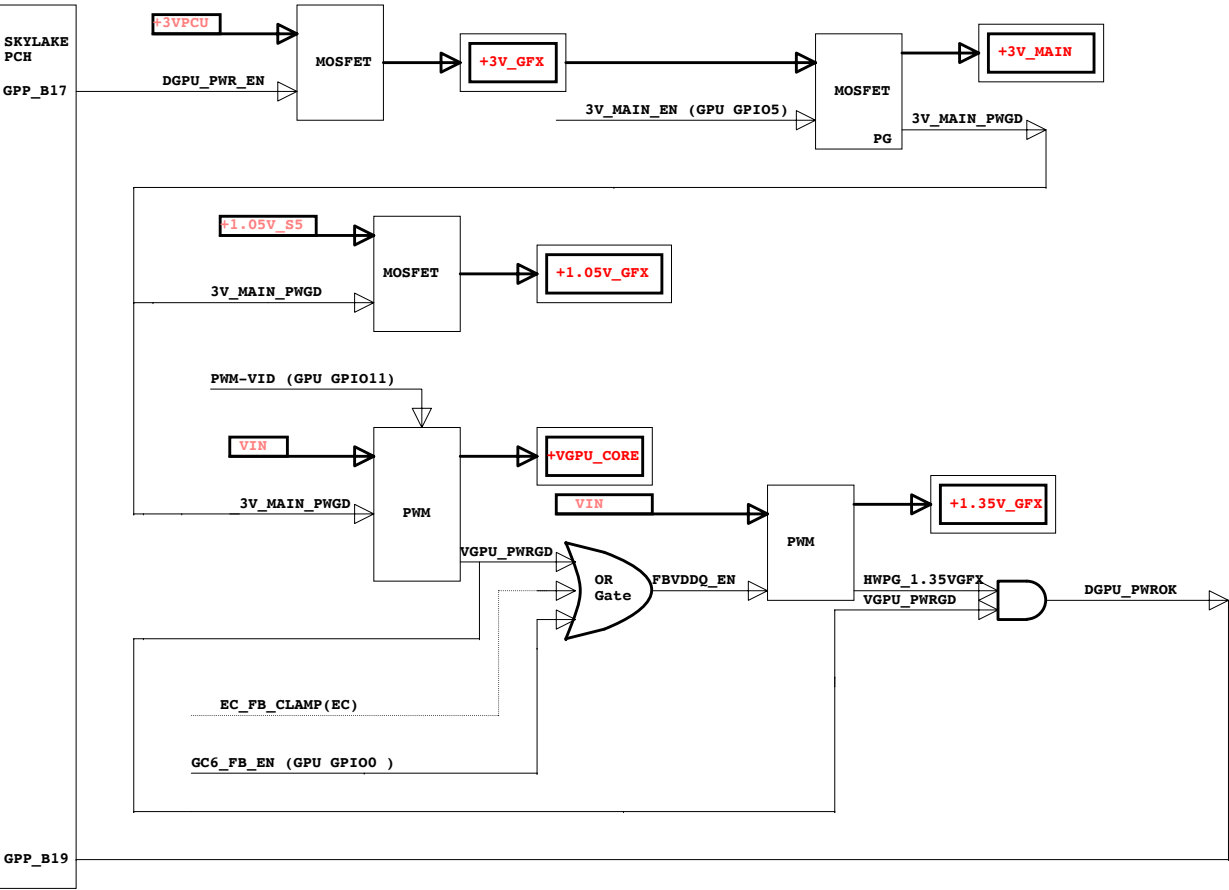
Check PU High with HW side



+1.35V_GFX for GDDR5

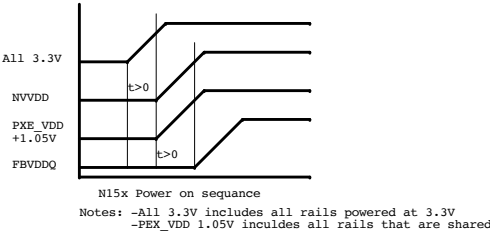
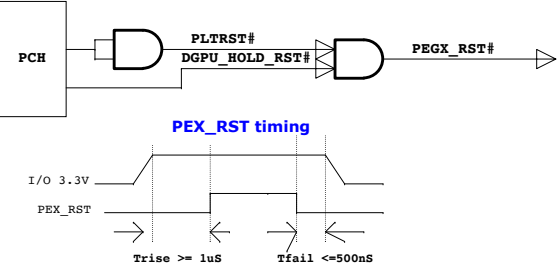


VGA power up sequence

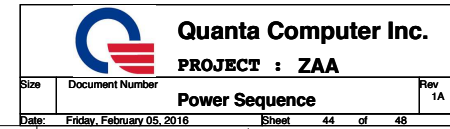


Power plane	Description	Voltage	S0	S3	S5
+VCCCORE	Core voltage for CPU	0.55~1.5	ON	OFF	OFF
+VCCGT	Voltage for on-Die VGA of CPU	0.55~1.5	ON	OFF	OFF
+VCCGTX	Voltage for on-Die VGA of CPU	0.55~1.5	ON	OFF	OFF
+VDDQ_VTT	0.6V switched power rail for DDR4 terminator	0.6	ON	ON	OFF
+VDDQ	0.6V switched power rail for DDR4	0.6	ON	ON	OFF
+VCCSA	Voltage for system agent of CPU	0.55~1.15	ON	OFF	OFF
+1.2VSUS	1.2V switched power rail for DDR4	1.2	ON	ON	OFF
+1V_S5	1V switched power rail	1	ON	ON	ON
+1V_SUS	1V switched power rail	1	ON	ON	OFF
+VCCIO	Voltage for I/O of CPU	1	ON	OFF	OFF
+VCCOPC	Voltage for on package cache of CPU	1	ON	OFF	OFF
+2.5V_SUS	2.5V switched power rail for DDR4	2.5	ON	ON	OFF
+1.8V_S5	1.8V switched power rail	1.8	ON	ON	ON
+1.5V	1.5V switched power rail	1.5	ON	OFF	OFF
+3V_S5	3.3V switched power rail	3.3	ON	ON	ON
+3V_PCU	3.3V always on power rail	3.3	ON	ON	ON
+3V	3.3V switched power rail	3.3	ON	OFF	OFF
+5V_PCU	5V always on power rail	5	ON	ON	ON
+5V_S5	5V switched power rail for system	5	ON	ON	ON
+5V	5V switched power rail	5	ON	OFF	OFF
VIN	Adaptor power supply	19	ON	ON	ON
+2.5V	2.5V switched power rail for DDR4	2.5	ON	OFF	OFF
+3V_RTC	RTC power	3.3	ON	ON	ON
+VGPU_CORE	VGA power	0.6~1.2	ON	OFF	OFF
+1.05V_GFX	VGA power	1.05	ON	OFF	OFF
+1.35V_GFX	VGA power	1.35	ON	OFF	OFF
+3V_GFX	VGA power	3.3	ON	OFF	OFF
+5V_S5_V2	5V for Type-C source power rail	5	ON	ON	ON
+TYPEC_VBUS	5V Type-C power rail	5	ON	ON	ON

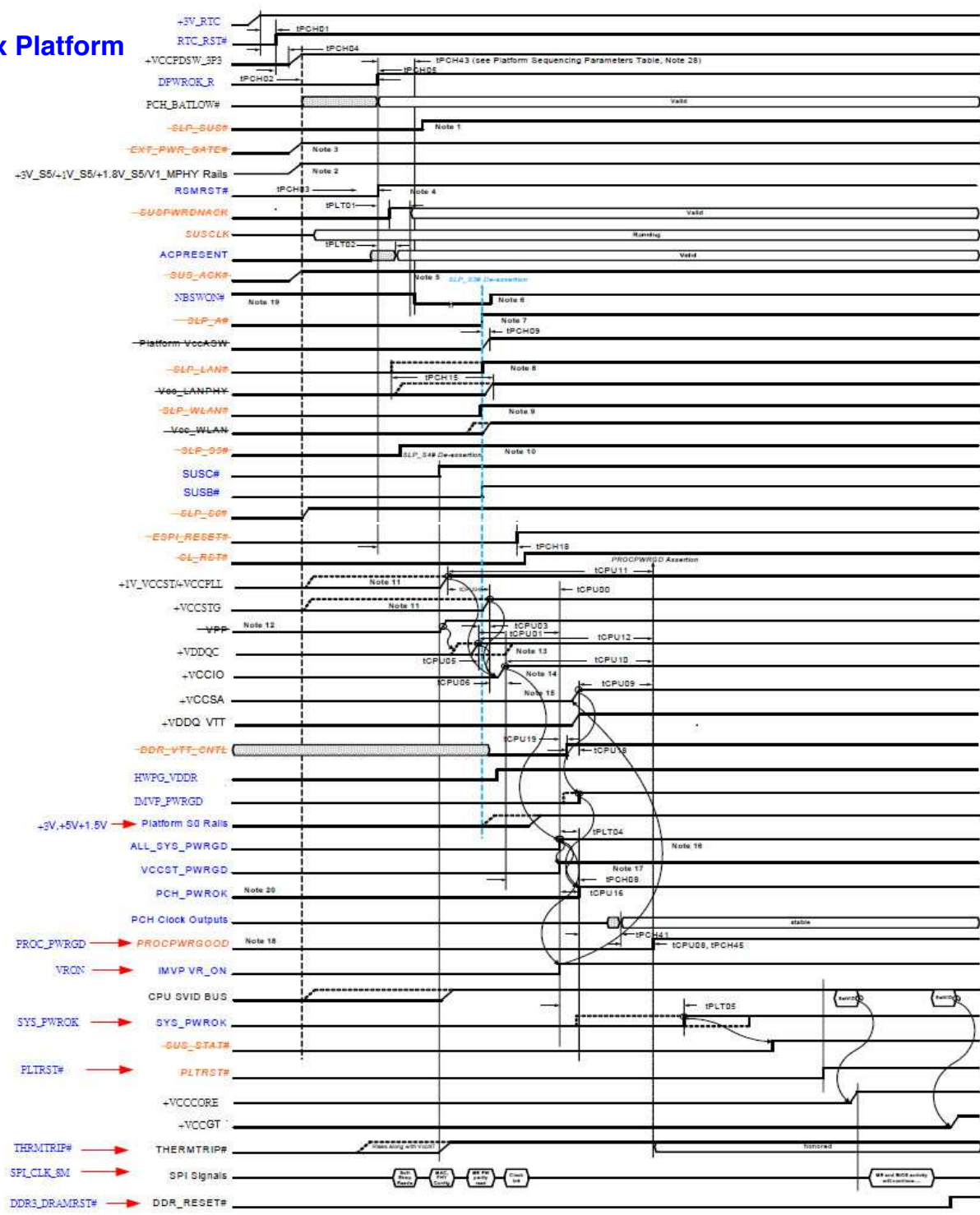
VGA Reset



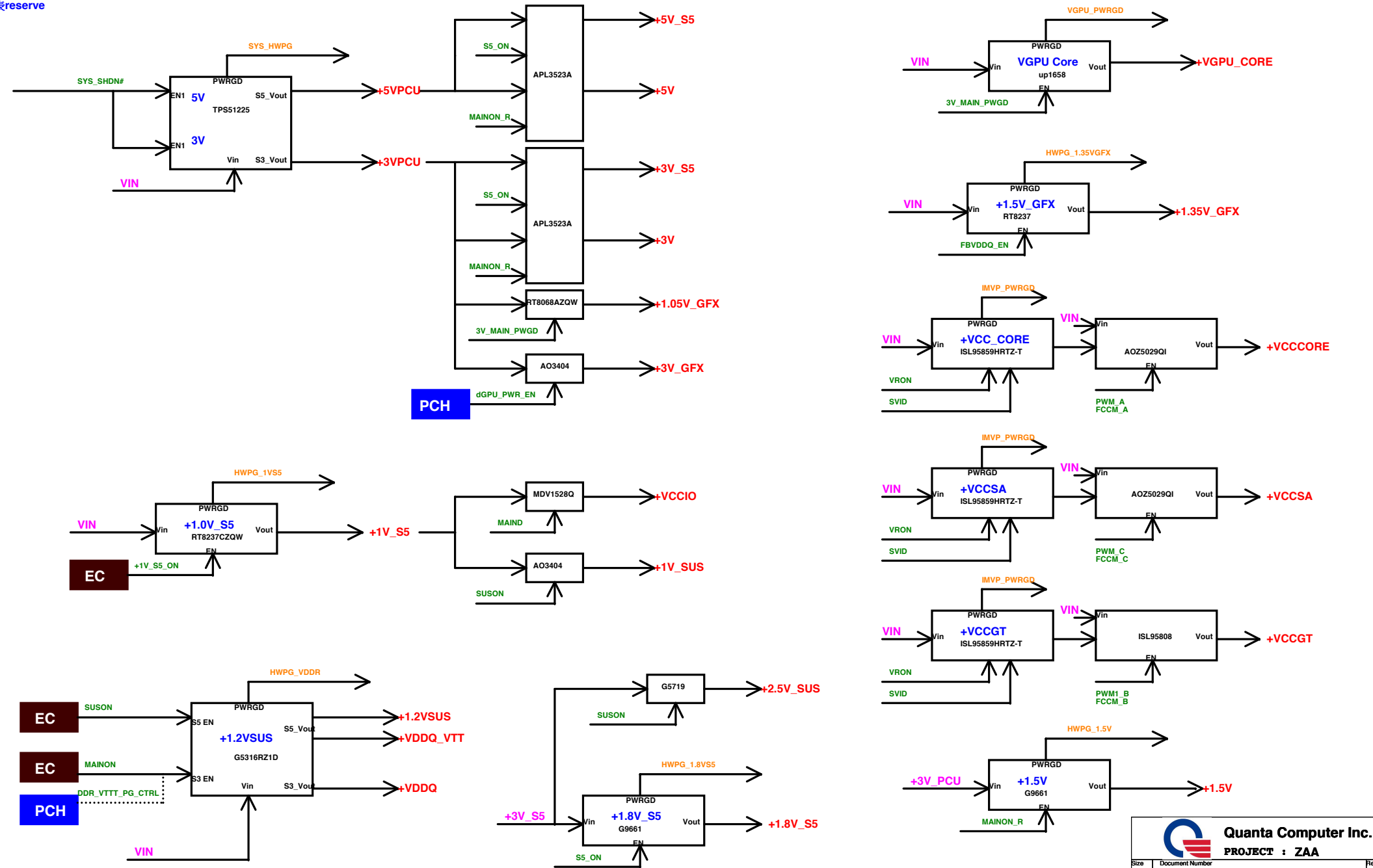
Non Deep Sx



Skylake U Non-Deep Sx Platform
Power on sequence

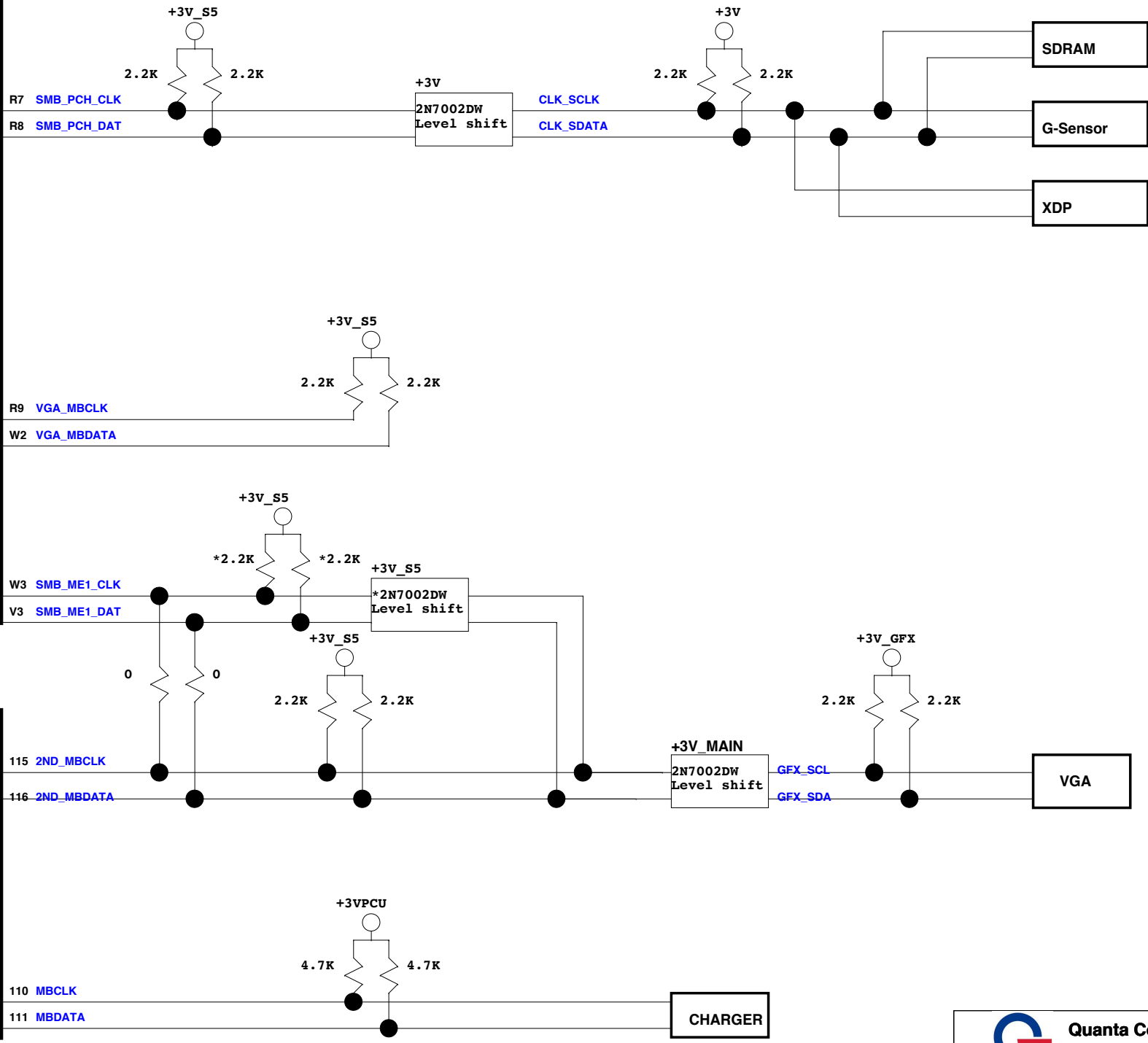


實線表default
虛線表reserve



Skylake U

EC
IT8987CX



Model

Date

CHANGE LIST

B-CHANGE

B0. Change FP from 0201 to 0402; C689,C688,C683,C194,C241,C227,C216,C242,C205,C252 for RDC request.

B1. Change CN95, CN6, CN20,CN2019, CN7,JDIM1, JDIM2,CN10 of foot-print

B2. Page 33 Mount PR6296, remove PR6295 for EC can't boot issue

B3. Page 12 Delete R11170, mount R11133 for DDR4's SPD

B4. Page 13 Delete R11174, mount R11134 for DDR4's SPD

B5. Page 27 Change POA IC U1006's P/N. (AL000103006)

B6. Page 28 Change CN23's P/N--- 5H; Reserve R11284

B7. Page 25 change R247 value from 0 to 2.2 Ohm (CS-2204FA00); Change R251, R262, R269, R11265 footprint from 0603 to 0805 (LAN)--(CS07504FA11)

B8. Page 2 Mount R485 for THRMTRIP#

B9. Page 17 Change R4314 & R4306 of value for KA/KB

B10. Page 6 Mount Q6060 for CMOS issue

B11. Page 31 Swap U45 Pin81 & Pin32 for DAC Fan; Add D4015 for ESD; Reserve R11282 for battery

B12. Page 6 R512 Change P/N from 58 to 1 % (CS22702FB14)

B13. Page 8 IOAC setting change into none IOAC R598 mount , R599 remove.

B14. Page 29 Delete R328,R11109,R327,R347,R346,C4716,C4718,C4717,C4558 & Q6061; Add C321,C723,C728,C719,R218 & U12 for DAC Fan; Change CN8's P/N

B15. Page 29 Change KB/BL connector CN's FP,P/N. (DPFC04FR111) & remove CN2018 for ME request

B16. Page 29 Chage CP1-CP6 into 0402 size, from C4788-C4811

B17. Page 26 Change Speaker connector CN18's FP,P/N. (DFHD04MR176)

B18. Page 26 Modify U16,U4512 pin2 to +3V , then off U16 & U4512

B19. Page 15 Change C4117,C4118 from 22U into 10U, and Add C4815, C4812 (10U-0402) for layout speace.

B20. Page 18 Change C4423,C4426 from 22U into 10U, and Add C4813, C4814 (10U-0402) for layout speace.

B21. Page 31 Change SW4's P/N & FP; Add R1283 for EC AUTO RECOVERY.

B22. Page 28 Change Hole16's P/N & FP, Add Hole25, Hole26 for ME modify ; Add R11284

B23. Page 5 Change C202 value from 47U to 22U & add C4816

B24. Page 23 Change R11268,R11271 from 33 to 47 Ohm ; Change L5,L6,L7's P/N; Not mount C718,C716,C319,C333,C336

B25. Page 32 Change PJ3's FP

B26. Page 30 Change U22's FP

B27. Page 24 Change CN12's FP

B28. Page 4 Change C739 from 10 to 22P & mount for EMI request

B29. Page 21 Add C4817 & C4818 for EMI request

B30. Page 2 Change R577 & R152 power to +3V_S5 for leakage

B31. Page 8 Change R211 power to +3V_S5 for leakage

B32. Page 22 Add R11285, R11286(reserve)

B33. Page 21 Cancle co-layout R11225,R11226,R11227,R11228,R11229,R11230,R11231 & R11232.

B34. Page 14 Change C356 & 362 for vendor recommend

B35. Page 24 Mount R11277, Remove R11274 change to -4db

Power-CHANGE

B36. Page 33 Delete JP18, JP20 ,PR248,PR249,PR6127,PR6219,PR345,PR244,,PR247,PR246,PR266,PR272

B37. Page 34 Delete JP9

B38. Page 35 Delete JP16

B39. Page 36 Delete JP22,JP29

B40. Page 37 Change PR225,PR224's value from 10k to 13.7K; Add SP@ at PR194,PR203,PR207,PR202

B41. Page 38 Delete JP24, change JP25 to PR6304

B42. Page 39 Delete JP26

B43. Page 40 Delete PR6298,PQ6066,PR137,PQ4,PR153,PQ10; Change PU2 & PU6's P/N for ESD.

B44. Page 41 Delete JP34

B45. Page 42 Delete JP10,JP35

B46. Change DDR solution to RT8231B

Change +1V_S5 solution to G5335

Change +1.35V GFX solution to G5335

Revise LDO P/N to AL001282000 (YB1282PSP8)

LDO (PU2 & PU6) Pin4 adding 1u/6.3

B47. Page 37 Change PC10, PC20, PR192,PC28,PR211,PR220 & PC39 of value.

B48. Page 25 Add R6308

C-CHANGE

C1. Change 0 Ohm to short pad & remove JP,

R11,R14,R15,R28,R66,R67,R11129,R102,R194,R224,R229,R235,R790,R791,R792,R11111,R11112,R11113,R11140,R112,R135,R179,R180,R182,R185,R187,

R188,R192,R193,R198,R240,R252,R11131,R164,R246,R339,R350,R11185,R11186,R550,R657,R718,R721,R782,R11153,R11283,R795,R796,R797,R816,

R817,R818,R819,R820,R821,R11196,R11199,R11202,R11207,R11279,R11280,R11281,R948,R951,R956,R958,R959,R960,R11061,R11062,R11110,R11133,

R11134,R11136,R11137,R11138,R11139,R11141,R11253,R11254,R11255,R11256,R11267,R11270,PR257,PR263,PR267,PR274,PR281,PR82,PR83,PR94.

PR87,PR254,PR264,PR109,PR110,PR117,PR122,JP8,JP10,JP14,JP15,JP17,JP22,JP33,JP19,JP21

R4328,R4335,R2855,R2870,R318,R221,R403,R405,R742,R743,R725,R745,L19,R2872

C2. Page 31 remove SW2 -- power bottom

C3. Page 29 Change CN20 & CN2019 K/B connector of P/N

C4. Page 27 Delete Q76, R11288; Add C4819, R11290 ,R11291,R11298,R11299,R11302,R11303,R11300,R11301,R11292,R11293,R11294,R11295 for co-layout POA & PBA ; Reseeve EC52,EC53,R11289 & R11287


C5. Page 21 remove R11193, double mount at type-C

C6. Page 32 for power request change short pad to 10 Ohm, location PR209 & PR210; Change PC115 of value

C7. Page 8 remove R618, it can't mount, because none device.

C8. Page 38 mount PC138 -- power request.

012_001_P0132



Quanta Computer Inc.

PROJECT : XAA

Change list

Doc No.

Doc Name: 012_001_P0132

DOC NO.

PROJECT MODEL :ZWA

APPROVED BY:

PART NUMBER:

DRAWING BY:

DATE:

REVISION: